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Comparison between Conventional Ripple Carry Adder and Reversible Ripple Carry Adder Using Peres Gate and HNG Gate

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----------***ABSTRACT***----------
Reversible logic plays an important role in quantum computing to synthesis in electric circuits. In modern systems, power dissipation is high due to continuous switching of inbuilt components. In present generations, the difficulty of chips is increasing as more number of components or devices is fabricated on a single chip. Due to high density of disk, the power consumption is high. To reduce power consumption alternate method is power optimization method. The important method to achieve the optimization in power is by using reversible logic. It can be developed by low power CMOS technology .the reversible logic can be proposed for reducing quantum cost. It produces garbage outputs. In this paper we are implementing the 16 bit reversible ripple carry adder using Peres and HNG gate .
KEYWORDS: quantum computing, Peres gate, garbage outputs, adder design, reversible logic.

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I INTRODUCTION

In this process thereversible computation can be done to someextent. It uses deterministic transitions from one state to another state. An obligatory condition for reversibility is the relation between the inputs and outputs of non-zero probability to their substitute inputs must be similar to their outputs. It is in the form of unconventional computing [1-2]. The most closely related types of reversible computing is based on the physical performance of the device and the logical performance of the device.

1.1 Physical reversibility: A process is said to be physically reversible if there is no increase in physical property. In a non deterministic process the relation depends on past and present states is not a single valued function. Thisimplementation controls and characterizes the physical dynamics of mechanisms to carry out the arithmetic operations. Each logical operationaccumulate anirrelevantamount of mechanism in its physical state, else the arithmetic operations can be carried out by active energy and the majority energy is retained and reused for any physical operations [3]. In present days, a wide variety of reversible device concepts, logic gates, electronic circuits, processor architectures, have been designed and analysed .

1.2 Logical reversibility: Before implementation one should identify its limits and the cost that can assigned in gate levelcircuits. In this reversible logic, the NOT gate is irreversible because it can be done in conventional logic [4]. The XOR gate is irreversible because its two inputs cannot be uniquely reconstructed from its single output. However, a reversible version of the XOR gate the CNOT controlled NOT—can be defined by preserving one of the inputs. The three-input variant of the CNOT gate is called the toffoli gate consider a, b as two inputs and c would be the third input. (c is XORed with (a&b)) with c=0. Whichgives AND function, i.e.,a.b=1. Thus, the Toffoli gate is universal and can implement any reversible and can be implemented by any Boolean function [4].(Given enough zero-initialized ancillary bits). More generally, reversible gates that consume their input have no more inputs than outputs. A reversible circuit connects reversible gates without fan outs and feedbacks. Therefore, each circuit contains an equal number of input and output wires. It has been observed that for every bit of information loss in logic computation that are not reversible. A gate is considered as a reversible only if for each defined input there is a defined output [5]. A reversible logic is having same number of inputs and same no, of outputs. This circuits can perceive only balanced functionsandunbalanced functions can be considered as garbage outputs .

1.3 Advantages:

- It usesa minimum number of garbage outputs.
- It uses a minimum number of reversible gates.
- It usesa minimum constant inputs.

II LITERATURE SURVEY:

It is not possible to realize quantum computing without implementation of reversible logic. To implement a reversible logic function one should know the basic and important definitions .

Garbage outputs: garbage output is defined as an unwanted output data without affecting its input data

Reversible function: Boolean functions are irreversible $F(x_1,x_2 \ldots x_n)$ only when number of inputs and outputs are equal. And any output pattern has a unique one to one mapping between inputs and outputs .

Gate count: The gate count is major cost metric in the evaluation of reversible circuit .

Delay: he delay of the circuit depends on the number of gates involved in the operation .

Quantum cost: the total number of gateswhich realizes the given function is also known as quantum cost. It varies depend on number of inputs and outputs of gates .

2.1 Some of the basic reversible logic gates :

(a). Feynman gate: The basic 2*2 Feynman logic gateis shown in the below fig 1.It is having 2 inputs (A, B) and 2 outputs(P=A, Q=A^B). The working function is shown in the below Table 1

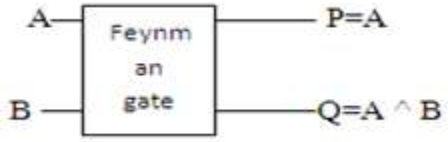

Fig 1: Feynman gate

A	B	P=A	Q=A^B
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table1: Truth table of Feynman gate

(b). Fred kin gate: Is a 3 bit gate that swaps the last two bits if the first bit is 1, i.e., a controlled swap operation. It is having 3 inputs(A, B, C) and 3 outputs (P=A, Q=A'B ^ AC, R=AB ^ A'C. to understand the working of fredkin gate refer the truth table as shownin Table 2. The basic structure can be shown fig 2

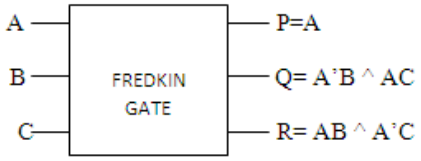

Fig 2: Fredkin gate

A	B	C	P=A	Q=A'B ^AC	R=AB ^A'C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	1	1

Table 2: Truth Table

(c). Peres gate: it is a 3*3 gate which is having three inputs (A, B, C) and three outputs (P=A, Q= A^B, R= AB ^ C shown in fig (3). Working can be explained in truth table .

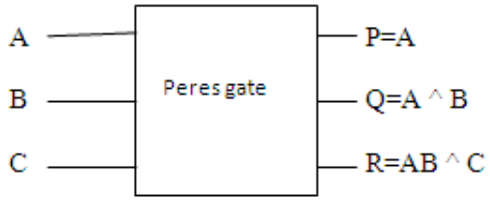

Fig 3: Peres gate

A	B	C	P=A	Q=A^B	R=AB^C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Table3: truth table for Peres gate

(d). HNG gate: it is a 4*4 reversible gate. It is having 4 inputs(A,B,C,D) and 4 outputs (P=A, Q=B, R= A ^B^C, S=(A^B).C^AB^D is shown in fig (4) and working can be explained by truth table in table 4.

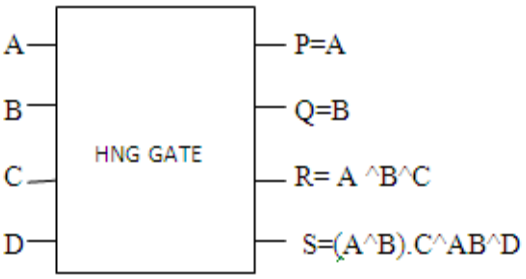

Fig 4: HNG Gate

A	B	C	D	P=A	Q=B	R=A^B^C	S=(A^B) .C^AB^D
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	1	1
0	1	1	1	0	1	1	0
1	0	0	0	1	0	1	0
1	0	0	1	1	0	1	1
1	0	1	0	1	0	1	1
1	0	1	1	1	0	1	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	0	0
1	1	1	0	1	1	0	1
1	1	1	1	1	1	0	0

Table 4: Truth Table for HNG gate

III PROPOSED METHOD:

In the proposed method we design and compared the reversible ripple carry adder with conventional ripple carry adder. We are using different reversible gates to design ripple carry adder using Peres gateand HNG gate .

Peres gate:

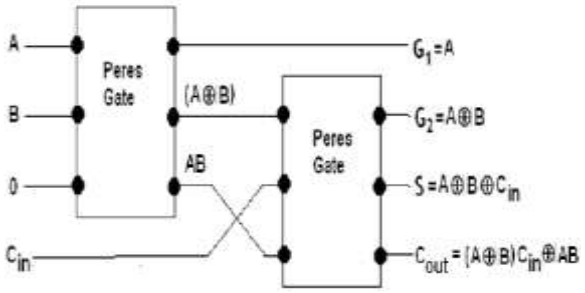

Fig 5: 1 bit Peres gate

Full adder is a circuit which is used to perform arithmetic operations the output equations can be written as
Sum=A⊕B⊕Cin
Cout= (A⊕B) Cin⊕AB
G1= A
G2= A⊕B

Using two 3*3 Peres gates the output of the reversible logic circuit consists of two garbage values and one constant input with an efficient quantum cost is shown in fig 5 .

Design of 16 bit ripple carry adder using Peresgate: The full adder is a block of ripple carry adder which includes binary full adder .In the ripple carry adder circuit for the first full adder block we are giving three inputs (A0, B0, Cin) , the third input Cin=0. The block diagram of four bit ripple carry adder using Peres gate is shown below. For implementing a 16 bit reversible ripple carry adderis shown in fig(7) 32 Peres gates are needed. Hence the total gate count for four bit Ripple carry adder is 8.Therefore to construct a 16 bit ripple carry adder 32 Peres gates are required [7].

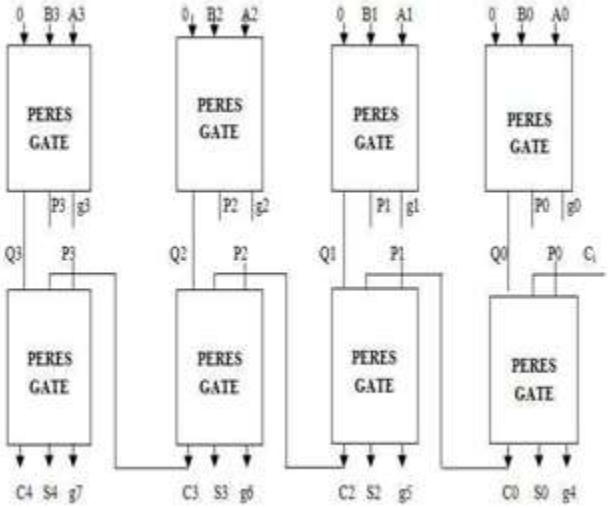

Fig 6: 4 bit ripple carry adder

The block diagram of four bit ripple carry adder using HNG is shown in Fig for constructing a four bit reversible ripple carry adder using HNG, 4 HNG are essential. Hence the total gate count for four bit Ripple carry adder is 4. Therefore to construct a 16 bit ripple carry adder 16 HNG are Needed[8].

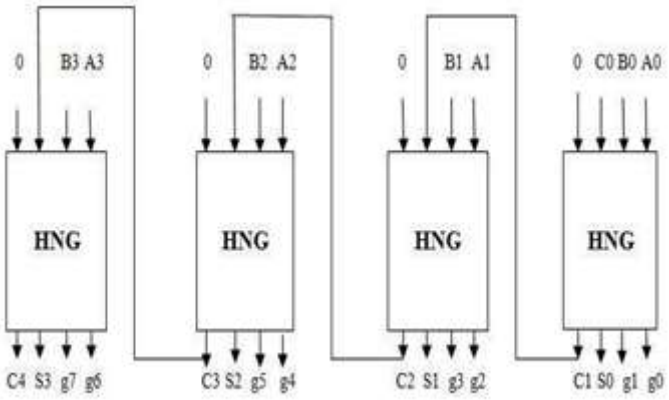

Fig 7: 4bit ripple carry adder using HNG gate

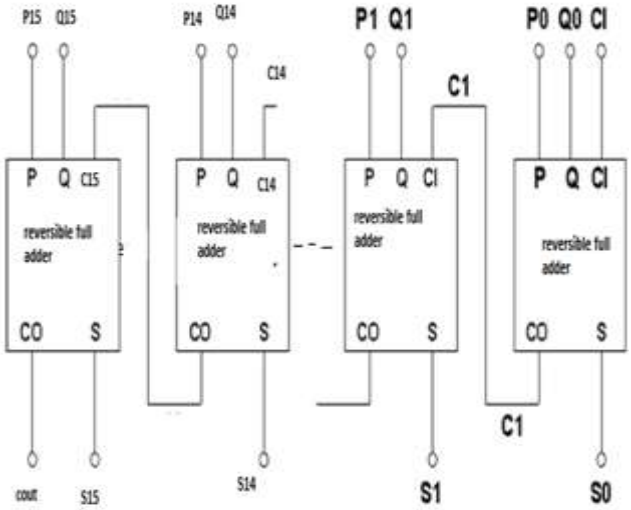

Fig 8: proposed 16 bit reversible fulladder

IV RESULTS AND DISCUSSIONS:

The proposed Peres ripple carry adder is implemented and resulted by using Verilog and simulated in Xilinx 9.2 I.The output waveform for 16 bit and 4 bit reversible ripple carry adders is shown in below fig 8.

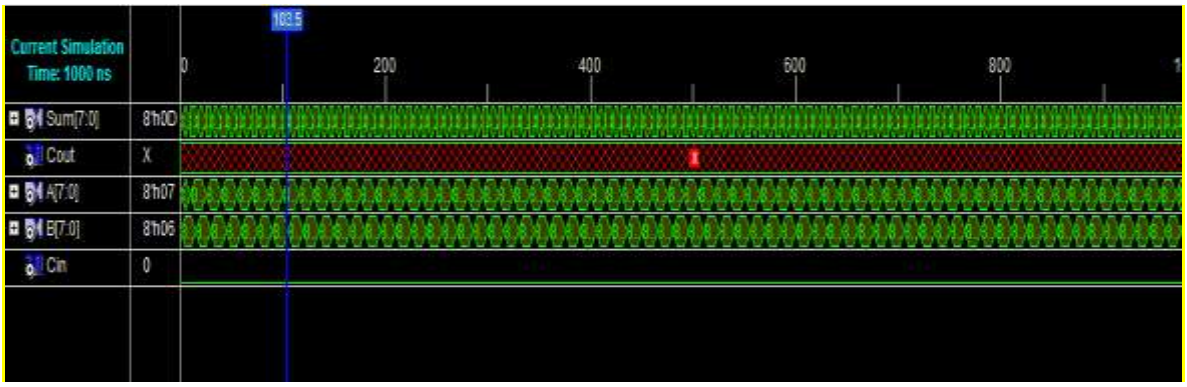

Fig 9:Simulation results for 4 bit ripple carry adder

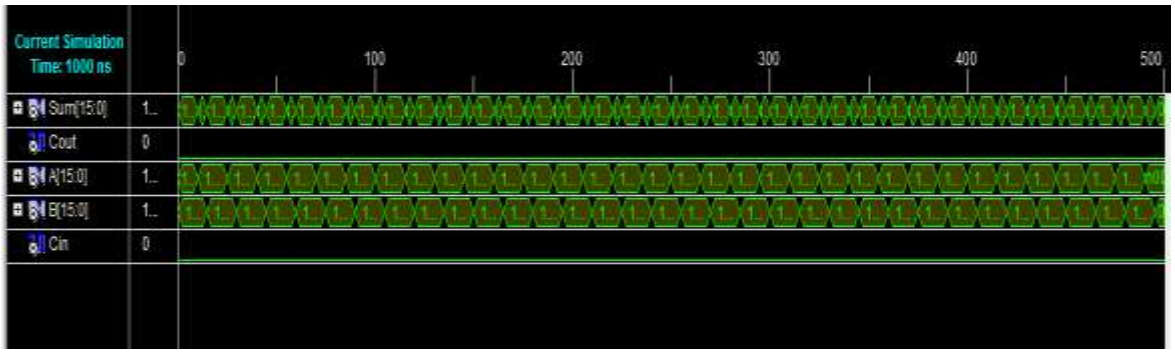

Fig 10:Simulation output for 16 bit ripple carry adder

The comparison of two reversible Ripple Carry Adder based on three parameters i.e. Gate count, Garbage output and Quantum cost is shown in the table

Parameters	16 bit reversible adder using Peres gate	16 bit reversible adder using HNG gate
Gate count	32	16
Garbage output	32	32
Quantum cost	128	96

Table 5:Comparison between Reversible Ripple Carry Adders

V CONCLUSION

This paper presents the design and simulation of 16 bit reversible ripple carry adder using Peres gate and HNG gate. The power delay is calculated for 16 bit reversible ripple carry adder. Also, the time delay between conventional ripple carry adder and reversible ripple carry adder using Peres gate and HNG gate was found, 8.16ns, 7.79ns, and 7.76ns

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