Design of Fractional-N Phase Locked Loop for X-Band Frequency

[1]saeed Talati, [2]mohammadi-Ali Baheri-Fard, [3]houman Akbarzadeh

[1,3]*Electrical Engineering Department, Shahid Sattari Aeronautical University*
[2]*Electrical Engineering Department, Sahand University of Technology*
Corresponding author: saeed Talati

--ABSTRACT--

This paper presents a fully integrated Fractional-N phase locked loop (Frac-N) to cover the X-band frequency. In this paper a new linearization technique is proposed in the Charge Pump (CP) circuit. The Frac-N is implemented in the circuit level in 180-nm CMOS standard. Simulation result shows that the CP's currents are well matched and the maximum mismatch is around 0.4 μA in the Vctrl ranging of 0.2-1.6 V. Simulated phase noise of the Frac-N shows that the close-in phase noise at offset frequencies of 1 KHz, 10 KHz, and 100 KHz for when the technique is OFF are -40 dBc/Hz, -77 dBc/Hz, and -82 dBc/Hz, respectively, and when the technique is ON are -63 dBc/Hz, -88 dBc/Hz, and -96 dBc/Hz, respectively. Power consumption of the designed Frac-N is about 20-mW with a single 1.8-V power supply.

Keywords *- Fractional-N phase locked loop, Charge pump, Phase noise, Linearization, X-band frequency.*

I. INTRODUCTION

In our life, the communication satellite technology is developing in variety applications such as; astronomy, weather forecasting, broadcasting, mapping and also widely will be used in the future smart applications such as HDTV and internet-via-satellite services. In the last decade, the integration of a system into a single chipset with the aim to area minimization, lowering cost and as well as power consumption has become a major research area.

The Programmable Local Oscillator (PLO) which its function is to carrier generation for up-conversion data from base-band to RF and down-conversion data from RF to base-band is a key building block in the transceivers. The PLO is often implemented by using a Voltage Controlled Oscillator (VCO) in a programmable Phase Locked Loop (PLL) and can be separated into two categories: Integer-N PLL (Int-N) and Frac-N. The channel spacing in the Int-N is limited to the reference frequency while in the Frac-N is not. However, the phase noise performance of the Frac-N is highly sensitive to non-linearity operation of the sub-circuits while the Int-N have a suitable phase noise. Our target in this paper is to design a fully integrated Frac-N for X-band frequency.

However, many research have been presented to introduce full integrated Frac-N in the literature. A CMOS Frac-N for 8-12 GHz frequency band was presented in [1]. As reported in the paper, the output of the Frac-N is differential and as we know the high speed transceivers are implemented as orthogonal architectural which they need to an in-phase and quadrature-phase in the LO. Another reported is a fully integrated dual-band CMOS Frac-N for WLAN standards [2]. As reported in the paper, a self-calibrated CP is introduced to suppress the close-in phase noise. However, as can be seen the introduced idea is difficult to implementation an also the Frac-N will be faced to stability issue. Also a Frac-N is presented to cover multi-standards IEEE 802.11 a/b/g/n [3]. In this paper a new switchable LPF is proposed to minimize the reference spurs. As can be seen in the simulation results section, the proposed idea minimized the reference spurs while it's leads to raises the close-in phase noise. As well known, the close-in phase noise severely limits the performance of the Frac-N.

However, in this paper a new linearization technique is introduced in the CP circuit to achieve a matched charge and discharge currents. The linearization technique helps the Frac-N to suppress close-in phase noise and also a constant dynamic loop. The paper is organized as follows; in Section II system level and frequency planning of the Frac-N is described. Section III presented the detail of the Frac-N building blocks. Section IV revels the simulation results and finally the conclusion is presented in Section V.

II. FRAC-N FREQUENCY PLANNING AND SYSTEM DESIGN

System-level of the proposed X-band Frac-N is presented in Fig. 1. The frequency range from 8 GHz to 12 GHz is required in order to cover the X-band frequency. To achieve this cover of frequency range, two Quadrature VCO (QVCO) as low-band (to cover 8-10 GHz) and high-band (to cover 10-12 GHz) are used in the

proposed architecture. As can be seen in Fig. 1, the output of the VCOs are applied to a multiplexer in order to select the desired band as LO output. Also the power supply of the VCOs are tacking as switchable in order to keep-on the desired VCO and keep-off the undesired VCO in which to decrease power consumption. The LO is applied to the chain of dividers that consist of a high speed analog divide-by-4 and a Multi Module Divider (MMD) which is controlled by a Digital Delta-Sigma Modulator (DDSM). The output of the MMD is applied to a TSCP-PFD in order to compares the divided VCO's output with a reference signal. The reference signal in our architecture is adopted by 40 MHz crystal. In the following the output errors detected by the TSPC-PFD are converted of voltage (V) to current (I) by using a CP. The CP in our architecture is linearized and enhanced the matching characteristic of the currents. Finally, the injected charges from the CP are applied to a 3rd order LPF to convert I to V again in order to frequency control of the desired VCO.
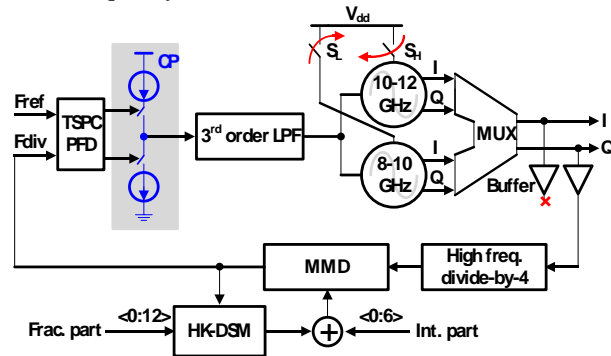

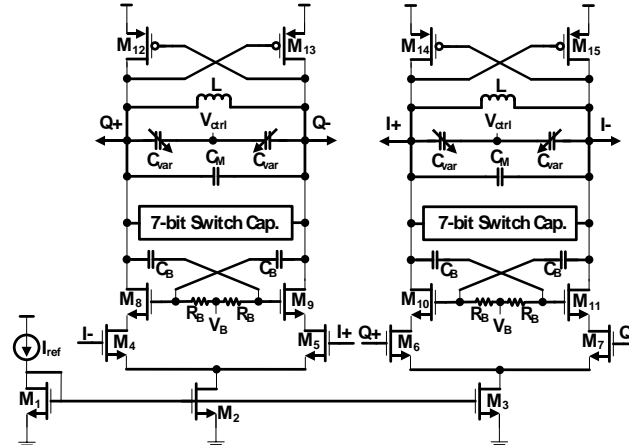**Fig.1. system schematic of the proposed X-band Frac-N**

Fig. 2. Circuit schematic of the proposed QVCO

III. FRAC-N BUILDING BLOCKS

VCO and Multiplexer

In our frequency planning two QVCO are designed to cover 8-10 GHz and 10-12 GHz as low-band QVCO (LB-QVCO) and high-band QVCO (HB-QVCO), respectively. The main circuit of these QVCOs is depicted in Fig. 2. As can be seen from Fig. 2, tank of the oscillators are based on a constant LC with a differential MOS-Varactor to adjust fine frequency tuning. Also, a 7-bit bank of switch capacitors are used to minimize the gain of QVCO and coarse tuning. The driver-circuit in these oscillators are implemented by using Nmos and Pmos cross-coupled pairs that they are biased by a tail-current for each one. The cross-coupled pairs are based on Class-C topology to achieve a proper noise performance and as well as high cover range [4]. In order to couple the differential oscillators, they are triggered each other by using series stacked transistors M4-7. The QVCO's outputs are applied to a 2-1 multiplexer in order to select desired band as LO signal. To save the power consumption, the multiplexer is designed based on pass-switch-MOS. The outputs of the multiplexer are connected to buffer in order to keep the full-swing amplitude and balance at the in-phase and quadrature-phase outputs.

High Frequency Divide-by-4

Since the frequency range of the X-band is so high, a high speed analog divide-by-4 divider is used as prescaler. Therefore, the differential outputs of the VCO are applied to a high speed analog divide-by-4. Fig. 3 shows the architecture's schematic of a high speed divide-by-2 circuit that two stage of them are series to achieve divide-by-4 [5]. This divider is a favorable technique which has potential advantages over conventional

NAND/NOR logic in terms of power dissipation, circuit delay, layout density and logic flexibility. As shown in Fig. 3, this divider consists of two same stage latches that they are coupled with together. In this architecture, the two NMOS/PMOS in the pull-down/pull-up network are used for latch/inputs-couple and M9, 10 in the differential output paths are used for switching (divider's input) and connection with differential outputs of the VCO.
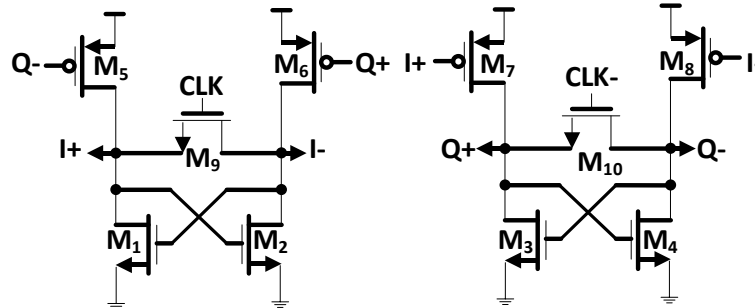

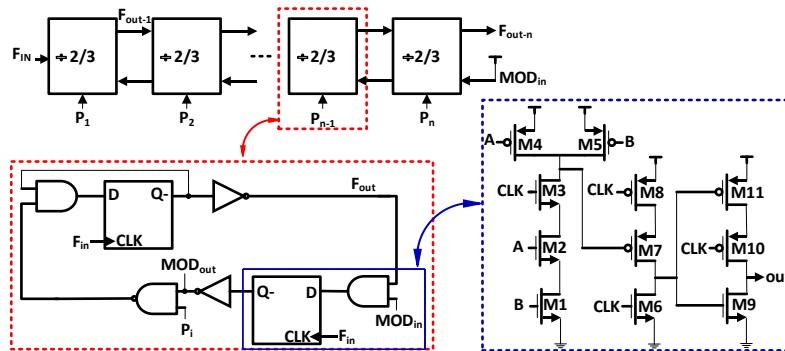**Fig. 3. Circuit schematic of the proposed analog divide-by-2**

Fig. 4. System and circuit schematics of the MMD

MMD

The modular dividers mainly classified in two categories; 1) Pulse Swallow Counter (PSC) and 2) MMD. In PSC architecture two additional counters are required for the generation of a given division ratio. Also in this architecture a feedback path from the output should be applied to the input and it leads to represent a substantial load on the output of the divider, so that power dissipation is increased. Besides, the additional design and layout effort required for the programmable counters increase the time-to-market of new products. The MMD structures is characterized by the absence of long delay loops, as feedback lines are only present between adjacent cells [6]. This "local feedback" enables simple optimization of power dissipation. Another advantage is that the topology of the different cells in the prescaler is the same, therefore facilitating layout work. The Multimode dividing block consists of a chain of dividers of 2/3 that the number of dividers used in this block is determined by the required divider range. The relation of this divisor is as follows,

$$N = 2^n + P_{n-1}.2^{n-1} + P_{n-2}.2^{n-2} + ... + P_1.2^1 + P_0.2^0 \qquad (1)$$

where, N, p, and n are represents the division ratio, control bits to enable divider to divide-by-3, and number of stages, respectively.

HK-MASH 1-1-1

Fractional divisions are realized by using an array of programmable dual-mode dividers, that they are controlled by using a Digital Delta Sigma Modulator (DDSM). According to [7] at the output of a first order modulator, SQNR, could be written as follow:

$$SQNR_{dB} = 10Log\frac{P_{sig}}{\delta_e^2} - 10Log\left(\frac{\pi^2}{3}\right) + 30Log\,(\text{OSR}) \qquad (2)$$

where $psig, \delta$, OSR are the power of the signal, variance of quantizer noise, and over sampling of the input signal, respectively. The *OSR* could be written as follow:

$$OSR = \frac{f_s}{2f_b} \qquad (3)$$

Where Fs, Fb are sampling frequency of the input signal and the input bandwidth of the modulator, respectively. According to (2), it is obvious that by increasing the frequency of the DDSM, OSR increases and as a result

SQNR increase. In other words, by increasing the operation frequency of the DDSM, the maximum noise of it is transferred to the higher frequencies, which result in close-in phase noise suppressing. Another point in the design of the DDSM that should be considered in addition to noise sources, is the absence of fractional tones in the output spectrum. In order to reach a smooth spectrum in the output of the DDSM, the maximum sequence length of the modulator should be large enough. Based on the Parseval theorem, for a short sequence length, fewer unwanted tones will be appeared in the output spectrum. As a result, the output power is distributed on a few number of tones, which result in power increasing per tone. A conventional DDSM can be implemented by using of multi stage of Error Feedback Modulator (EFM) that are known as MASH 1-1 or MASH 1-1-1. The maximum sequence length for a MASH 1-1-1 is 2^{N+1}, where N is the number bits of the modulator. Recently a new structure of DDSM is presented that called HK-MASH, which in it the EFM model is modified. In this structure the maximum sequence length expanded to 2^{3N}. In this paper a HK-MASH 1-1-1 with 13-bit resolution is implemented for two reasons; 1) HK-MASH structure have a large enough sequence length that guarantees the power per tones is suppressed in the output spectrum, 2) 13-bit resolution have a simple structure to implementation of EFM. Fig. 5 presented the system level structure of the DDSM [7].
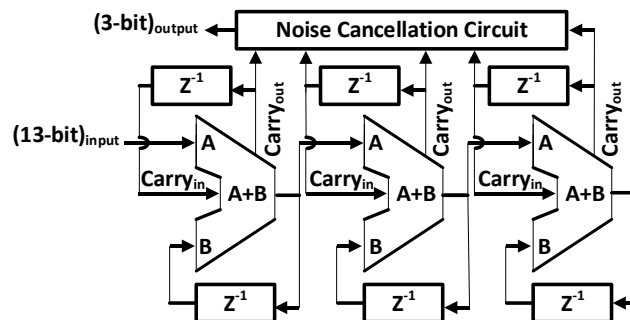

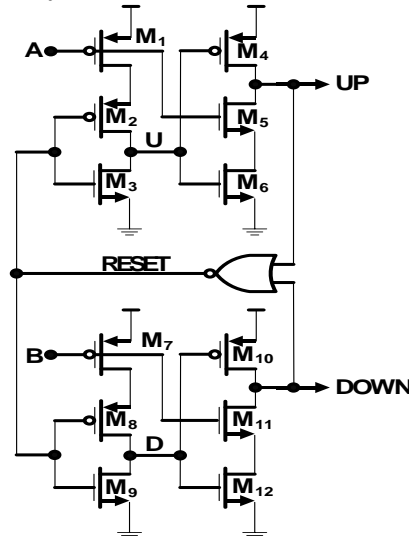**Fig. 5. System level architecture of the DDSM**

Fig. 6. Circuit schematic of the TSPC-PFD

TSPC-PFD

In this paper, we used of a PFD based on the TSPC topology that is depicted in Fig. 6. This structure is suitable to achieve simple implementation, high speed and low power consumption. Circuit operation is as follows: A rising edge on A (B) turns on M_5 (M_{11}), discharging the *UP* (*DOWN*) output. Once both *UP* and *DOWN* are low, *RESET* rises, discharging nodes U and D and forcing *UP* and *DOWN* to go high. M_3 (M_9) is placed in the D flip-flop in order to avoid short circuit for in case of A (B) is low and *RESET* is high that helps to reduce power consumption of the PFD [8].

New Linearized CP

As illustrated in Fig. 7, the charging (discharging) current is generated through the mirroring of current from M3 (M1) to M4 (M2). Let us to analyze the CP's operation in the range of 0-1.8 V; when the output voltage of the CP (that is dropped on the drain of M4 and M2) is in the range of 0-0.9 (0.9-1.8) V, M4 (M2) is in the saturation region while M2 (M4) is NOT and in this case, the conventional CP have not a proper discharging (charging) current network and this current will be dropped by decreasing (increasing) output voltage from 0.9 V to 0 V (1.8 V).

Therefore, we applied a current compensator for each current network (charging/discharging network). As illustrated in Fig. 7, we used of two current compensators ICh+ and IDis+ for ICh and IDis, respectively. As can be seen in Fig. 7, ICh+ (IDis+) is realized by Mf4 (Mf1) that it's current is mirrored to the charging (discharging) network. This time, let us to analyze the CP's operation for the new structure as is performed for the conventional CP. When the output voltage of the CP increases (decreases) from 0.9 V to 1.8 V (0 V), ICh (IDis) drops while ICh+ (IDis+) is starting to generate current, in order to compensate the total charging (discharging) current (ICh, tot (IDis, tot)). As a result, the lack of ICh (IDis) is compensated by ICh+ (IDis+). This operation of the linearized CP is revealed in Fig. 8. It should be noted that ICh+ and IDis+ are depended on the aspect ratio of Mf4 and Mf1, respectively. Therefore, we suggested that the size of Mf4 and Mf1 should be swept by the simulation tools to define a proper aspect ratio, in which to achieve fine compensations for charging and discharging current networks.
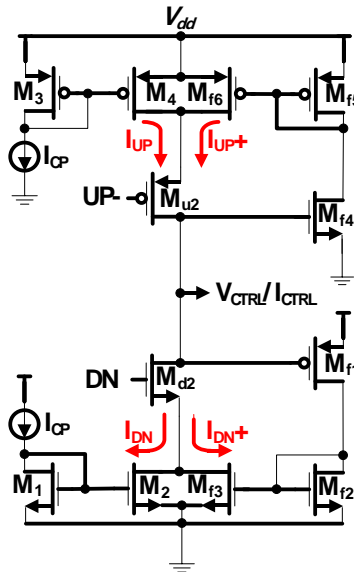

Fig. 7. Circuit schematic of the proposed new linearized CP

IV. SIMULATION RESULTS

The proposed Frac-N is designed in circuit-level by using Cadence-Virtuoso CAD-tool in 180-nm CMOS technology. The CP's characteristic is presented in Fig. 8. As can be seen from Fig. 8, the proposed technique linearized and matched the charging and discharging currents perfectly and the maximum current mismatch is around 0.4 µA in the Vctrl ranging of 0.2-1.6 V. To validate the ability of the proposed technique on suppressing the close-in phase noise of the Frac-N, Phase-Noise simulation is done and the result is presented in Fig. 9 for when technique is ON and OFF. As can be seen from the simulated phase noise of the Frac-N, the close-in phase noise at offset frequencies of 1 KHz, 10 KHz, and 100 KHz for when the technique is OFF are -40 dBc/Hz, -77 dBc/Hz, and -82 dBc/Hz, respectively, and when the technique is ON are -63 dBc/Hz, -88 dBc/Hz, and -96 dBc/Hz, respectively. Also the power spectral density of the designed Frac-N is presented in Fig. 10 and as can be seen the higher fractional spurs is lower than the carrier signal by role of 53 dBc. Power consumption of the designed Frac-N is about 20 mW with a single 1.8 V power supply.
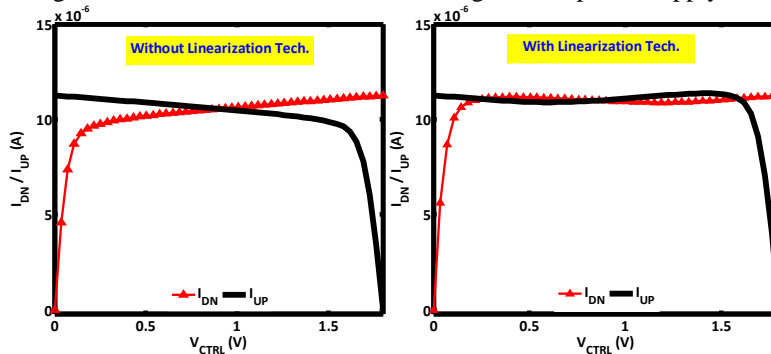

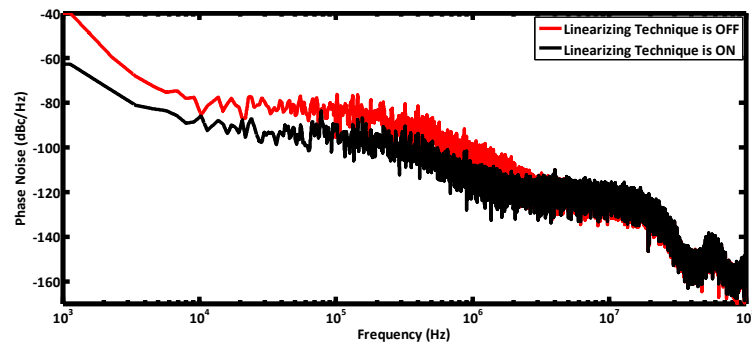**Fig .8. CP's characteristic for when the linearized technique is ON and OFF**

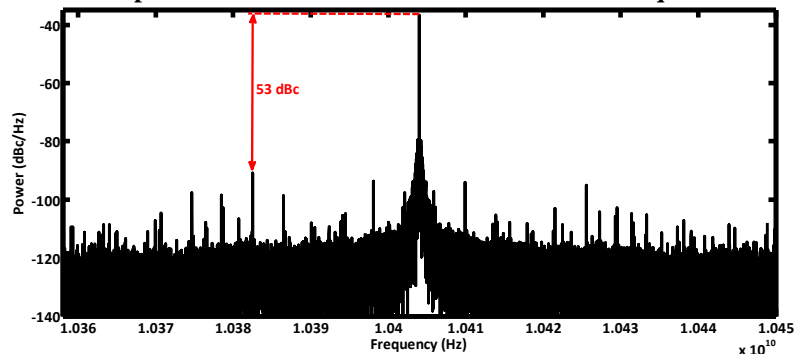**Fig. 9. Simulated phase noise of the Frac-N for when the technique is ON and OFF**

Fig. 10. Power spectral density of the designed Frac-N when the technique is ON

V.CONCLUSION

This paper presents a fully integrated Frac-N to cover the X-band frequency. In this paper a new linearization technique is proposed in the CP circuit to achieve a linear and matched charging and discharging currents in order to suppress the close-in phase noise of the whole Frac-N and as well as to have a constant dynamic loop in a wide range of the V_{ctrl} of the VCO. The Frac-N is implemented in the circuit level in 180-nm CMOS standard. Simulation result of the designed new linearization technique shows that the CP's currents are well matched compared with the CP without the technique and the maximum mismatch is around 0.4 µA in the Vctrl ranging of 0.2-1.6 V. The Frac-N is simulated by using Cadence-Virtuoso CAD-tool to validate the ability of the proposed technique on the close-in phase noise suppression and also to extract the other important specification. phase noise simulation is performed for the Frac-N and the results show that the close-in phase noise at offset frequencies of 1 KHz, 10 KHz, and 100 KHz for when the technique is OFF are -40 dBc/Hz, -77 dBc/Hz, and -82 dBc/Hz, respectively, and when the technique is ON are -63 dBc/Hz, -88 dBc/Hz, and -96 dBc/Hz, respectively. Power consumption of the designed Frac-N is about 20 mW with a single 1.8 V power supply.

REFERENCES

[1]. Avanji, Izadi, and Seyed Amin. "An Integrated 8-12 GHz Fractional-N Frequency Synthesizer in 90-nm CMOS." *The Modares Journal of Electrical Engineering* 16.2 (2016): 15-19.
[2]. Azadbakht, Mostafa, Ali Sahafi, and Esmaeil Najafi Aghdam. "A Dual Band Fractional-N Frequency Synthesizer with a Self-Calibrated Charge Pump for WLAN Standards." *Journal of Circuits, Systems and Computers* (2017): 1850131.
[3]. Azadbakht, Mostafa, Ali Sahafi, and Esmaeil Najafi Aghdam. "Low power fractional-N frequency synthesizer for IEEE 802.11 a/b/g/n standards in 90-nm CMOS." *Electrical Engineering (ICEE), 2016 24th Iranian Conference on*. IEEE, 2016.
[4]. Mazzanti, Andrea, and Pietro Andreani. "Class-C harmonic CMOS VCOs, with a general result on phase noise." *IEEE Journal of Solid-State Circuits* 43.12 (2008): 2716-2729.
[5]. Fard, Ali, and Denny Aberg. "A novel 18 GHz 1.3 mW CMOS frequency divider with high input sensitivity." *Signals, Circuits and Systems, 2005. ISSCS 2005. International Symposium on*. Vol. 2. IEEE, 2005.
[6]. Vaucher, Cicero S., et al. "A family of low-power truly modular programmable dividers in standard 0.35-/spl mu/m CMOS technology." *IEEE Journal of Solid-State Circuits* 35.7 (2000): 1039-1045.
[7]. Hosseini, Kaveh, and Michael Peter Kennedy. "Maximum sequence length MASH digital delta–sigma modulators." *IEEE Transactions on Circuits and Systems I: Regular Papers* 54.12 (2007): 2628-2638.
[8]. Lee, Won-Hyo, Jun-Dong Cho, and Sung-Dae Lee. "A high speed and low power phase-frequency detector and charge-pump." *Design Automation Conference, 1999. Proceedings of the ASP-DAC'99. Asia and South Pacific*. IEEE, 1999.