# Low-Complexity Shift Register Based on Decoder Enabled Pulsed Latches

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--------------------------------------------------------**ABSTRACT**---------------------------------------------------------
*This paper proposes a low complexity shift register based on decoder enabled pulsed latches. Power consumption and Area reduction plays a major role in sequential circuit design. To reduce the area traditional flip-flops are replaced by pulsed latches. The timing problem of latches are solved by use of various non overlap delayed pulsed clock signals. Traditional shift register uses single pulsed clock signal for data transition, which consumes additional power. Here the single clock is divided into small number of pulsed clock and the shift register are combined by several sub shift registers. To reduce the area and power decoder enabled non overlap delayed pulsed latches are used in shift registers instead of conventional shift register used by flip-flops. Shift register is divided in to sub-shift registers and decoder enables each latch in sub-shift registers. This proposed shift register saves more than 24% of power and 78% of area compared to conventional shift registers using flip-flops.*

*Keywords: Decoder, Flip-flops, low power, pulsed latches, Shift registers.*
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## I.    INTRODUCTION

Nowadays, the power and area reduction are the important constrain in the technology world. In VLSI circuit technology needs a low power and area efficient circuit design for the digital system applications.  A shift register is the basic building block in a VLSI circuit. In digital circuits, a shift register is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the "bit array" stored in it, shifting in the data present at its input and shifting out the last bit in the array, at each transition of the clock input.

Shift registers are commonly used in several applications, some of them are mentioned. Shift registers are used in digital filters [2], communication receivers [3], and image processing ICs [4] and [6]. Nowadays, the size of the image data is increase due to the high demand for high quality image data so the word length of the shift register must be increases to process large image data in image processing ICs.  An image-extraction and vector generation VLSI chip uses a 4K-bit shift register [4]. A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register [5]. A 16-megapixel CMOS image sensor uses a 45K-bit shift register [6]. As the word length of the shift register increases, the area and power consumption of the shift register also increases so it becomes an important design consideration.

Flip flop can store a single bit of binary data i.e. 1 or 0.  But if it needs to store multiple bits of data, need multiple flip-flops.  As a single flip-flop is used one bit storage, n flip-flops are connected in an order to store n bits of data. In digital electronics, a register is a device which is used to store the information. Flip-flops are used in constructing registers. But it takes a large power and area, to reduce the power and area the large flip-flops are replaced by small flip-flops that are the pulsed latches [1]. To reduce the power, shift registers are designed using pulsed latches. The timing problem of pulsed latches is solved by using multiple non overlap delay circuit [1].

The rest of the paper is organized as follows: Section II describes the proposed shift register architecture, Section III presents the simulation and measured results, finally the section IV shows the conclusion of the work.

## II.    PROPOSED WORK

Latches and flip-flops are the building blocks of sequential circuits [1] and these can be built from logic gates, but flip-flops are built from latches i.e. latches are simple and small size circuit. One flip-flop and latch can store one bit of data. The main difference between the latches and flip-flops is that, a latch checks input continually and change the output whenever there is a change in input. But, flip-flop is a combination of latch and clock that

continuously checks input and changes the output time adjusted by the clock. Conventional Shift registers built using flip-flops are take more power and area. Byung-Do Yang introduce a shift register based on delayed pulsed latches are mentioned in [1] can reduce power and area. The proposed method is concentrated on power and area in Low power VLSI circuits applications.Figure 1 shows the architecture of proposed shift register using decoder enabled pulsed latch. In this method the proposed shift register is divided in to several sub-shift registers. This paper mentioned 16bit shift register split into 4 sub shift registers each has 4 bit length and each sub shift register has 4 latches. Input signal (IN) is applied to the first latch in the first sub shift register and the output are mentioned as $Q_1$-$Q_{16}$.
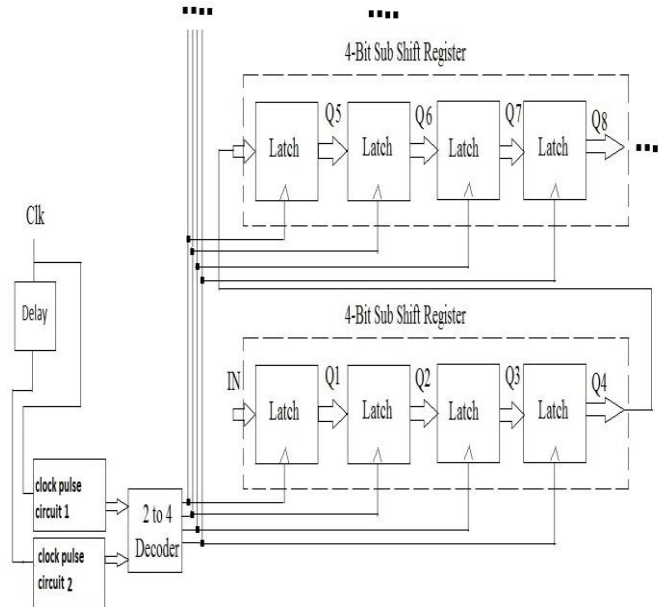


**Figure 1.**proposed shift register using decoder enabled pulsed latch

Enable signals are provided to each latch by delay pulse generator. In this arrangement reduces the number of delay circuits by substituting a delayed clock pulse generator using decoder is shown in figure 2. General 2:4 decoder is used for this proposed shift register as clock signal. Two clock pulse circuit are used where the main clock is applied directly clock pulse circuit 1 and connected after a delay to the clock pulse circuit 2. Clock pulse circuit consist of a delay, inverter and a AND gate, then output of the clock pulse circuit is connected to 2:4 decoder and get the output $D_0$,$D_1$,$D_2$ and $D_3$.
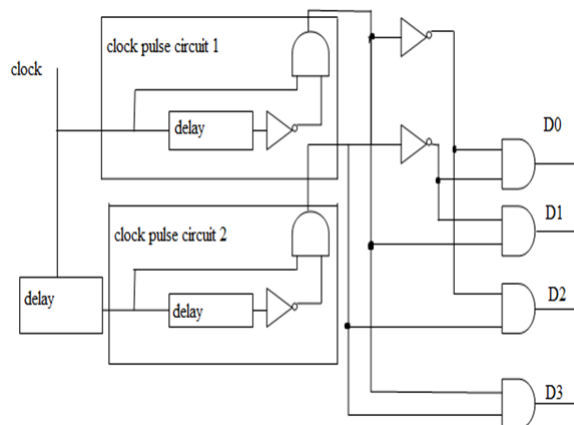


**Figure2.** Delayed clock pulse generator using decoder

In digital electronics, a binary decoder is a combinational logic circuit that converts a binary integer value to an associated pattern of output bits. Depending on its function, a binary decoder will convert binary information from n input signals to as many as $2^n$ unique output signals. In this application a decoder has 2 input and 4 outputs that combination is shown in table 1.

**Table 1:** Truth table of decoder

| $A_0$ | $A_1$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ |
|-------|-------|-------|-------|-------|-------|
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |

$A_0$ and $A_1$ are inputs And $D_0$-$D_3$ are outputs, both inputs are 0 then get $D_0$ as high, $A_0$ is 0 and $A_1$ is 1 then $D_1$ is high, $A_0$ is 1 and $A_1$ is 0 then $D_2$ is high and both inputs are 1 then get $D_3$ is high. These output are act as delayed clock pulse for the proposed shift register. The input of decoder, $A_0$ and $A_1$ signals are generated by the clock pulse circuits from the main clock.

SSASPL (Static differential Sense Amp Shared Pulsed Latch) technique [1], [7] is used for the implementation design of the proposed shift register. The basic circuit diagram of SSASPL is shown in figure 3. This method uses 7 transistors and it consumes low power. So because of this implementation design more power and area can be reduced.
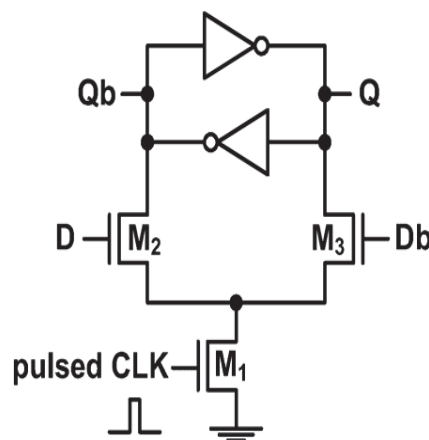


**Figure 3.** Simple circuit of SSASPL [1]

### III.    RESULT AND DISCUSSION

Proposed 16 bit shift register using decoder enabled latches are implemented using the SSASPL technology can reduce power and area.  Figure 4 shows the simulated output wave form of the proposed shift register based on decoder enabled pulsed latch. Modelsim SE is used for the simulation and Xilinx ISE is used for the area and power analysis.
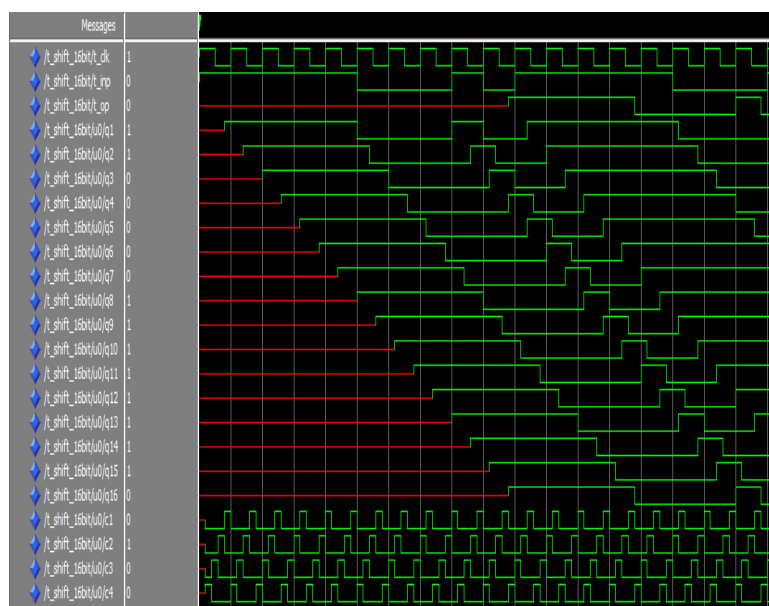


**Figure 4** simulated output wave form of proposed shift register

In the wave form $q_1$-$q_{16}$ shows the output of each latch and 'inp' signal is the input of the first latch 't_op' is the output of SISO shift register. $C_1$, $C_2$, $C_3$ and $C_4$ shows the clock that is corresponding to the output of decoder $D_3$, $D_2$, $D_1$ and $D_0$ respectively. $C_1$ ($D_3$) connected to the first latch in the each 4- bit sub-shift register and $C_4$ ($D_0$) is connected to the last latch in the each sub-shift register. Here $C_1$-$C_4$ occurs in one period of main clock. The comparison of conventional shift register using flip-flop, shift register with pulsed latches [1] and proposed method are mentioned in the table 1.

**Table 2** Power and Area comparison with conventional shift register.

| parameter | Shift register with flip-flops | Shift register with pulsed latches | Proposed shift register |
|---|---|---|---|
| Power(mW) | 136 | 114 | 104 |
| Area(gate count) | 136 | 32 | 30 |
| No of slice flip-flops | 15 | 3 | 2 |

From the comparison table 2, the proposed shift register based on decoder enabled pulsed latch can save more than 24% of power and 78% of area than conventional shift register using flip-flops.

## IV.    CONCLUSION

The proposed 16- bit shift register reduces the power and area consumption than the conventional shift register using flip-flops. The proposed shift register is constructed using pulsed latches, each latches are enabled using decoder. Here the 16 bit shift register is divided into 4 bit sub shift registers and the main clock is changed to delayed non-overlap multiple pulses that can solve the timing problem in the latches. The delayed clock pulses are generated using two clock pulse circuit and a 2:4 decoder it can reduce area and power more efficiently. This type of arrangement is less complex and simple than other conventional methods. It can save power and area more than 24% and 78% respectively compared conventional shift registers used by flip-flops and other pulsed latches methods.

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