Design of Combinational and Sequential Circuits Using Reversible Logic

P.Mamatha[1], K.Shirisha[2], T.Jyothsna[3]

[1]Senior Assistant professor , Aurora's technological and research institute, Hyderabad.
[2]Senior Assistant professor , Aurora's technological and research institute, Hyderabad.
[3] Associate professor , Aurora's technological and research institute, Hyderabad.

---**ABSTRACT**--
Reversible logic has become one of the most promising research areas in the past few decades and has found its applications in several technologies; such as low power CMOS, nanotechnology and optical computing. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs. The purpose of this paper is to give a frame of reference, understanding and overview of reversible gates .In this paper various logic gates and its applicability on logic design have been discussed. Also a brief framework of comparisons between various reversible circuits is presented on the basis of various parameters..
Keywords – Reversible logic, quantum cost, garbage ouputs.

I.   INTRODUCTION

Energy dissipation is one of the major issues in present day technology. Energy dissipation due to information loss in high technology circuits and systmes constructed using irreversible hardware was demonstrate by R.Landauer in the year 1960. According to Landauers Principle,the loss of one bit of information lost,will dissipate kT*ln(2) joules of energy where, k is Boltzmann's constant , T is the absolute temperature. In 1973, Bennet, showed that in order to avoid kTln(2) joules of energy dissipation in a circuit it must be built from reversible circuits. According to Moore's law the numbers of transistors will double every 18 months. Thus energy conservative devices are the need of the day. The amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Reversible circuits are those that do not lose information. The current irreversible technologies will dissipate a lot of heat and can reduce the life of the circuit. The reversible logic operations do not erase (lose) information and dissipate very less heat. Synthesis of reversible logic circuit differs from the combinational one in many ways. firstly, in reversible circuit there should be no fan-out, that is, each output will be used only once. Secondly for each input pattern there should be unique output pattern. Finally, the resulting circuit must be acyclic. Any reversible circuit design includes only the gates that are the number of gates, quantum cost and the number of garbage outputs

II.   RELATED WORK

Basic Definitions related to reversible logic
Reversible logic gate: Reversible Gates are circuits in which number of outputs is equal to the number of inputs and there is a one to one correspondence between the vector of inputs and outputs. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs
Constant inputs: This refers to the number of inputs that are to be maintaining constant at either 0 or 1 in order to synthesize the given logical function.
Garbage outputs: Garbage is the number of outputs added to make an n-input k-output function reversible. We use the words constant inputs to denote the present value inputs that were added to an (n:k) function to make it reversible. The following simple formula shows the relation between the number of garbage outputs and constant inputs. Input + constant input = output + garbage.
Quantum cost: Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. The quantum cost of a circuit is the minimum number of 2*2 unitary gates to represent the circuit keeping the output unchanged. The quantum cost of a 1*1 gate is 1 and that of any 2*2 gate is the same, which is 1

BASIC REVERSIBLE LOGIC GATES

1. FEYNMAN GATE:

Feynman gate may be a 2*2 one through reversible gate as shown in figure 1. The input vector is I(A,B) and also the output vector is O(P,Q) . The outputs area unit outlined by P=A,Q=A B. Quantum price of a nucleate physicist gate is one. Nuclear physicist Gate (FG) may use as a repetition gate. Since a fan out isn't allowed in reversible logic, this gate is helpful for duplication.
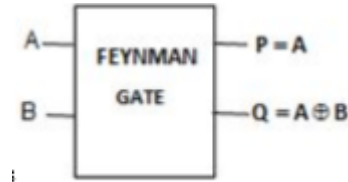

Figure.1

2. DOUBLE FEYNMAN GATE (F2G) :

Figure 2 shows a 3*3 Double Feynman gate. The input vector is I(A,B,C) an output vector is O(P,Q,R). The outputs are defined by P=A,Q=A B, R=AC.

Figure: 2

3. FREDKIN GATE:

Figure 3 shows a 3*3 Fredkin gate. The input vector is I(A,B,C) and the output vector is O(P,Q,R).
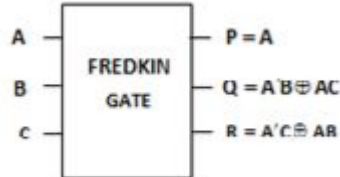

Figure 3

4. PERES GATE:

Figure 4 shows a 3*3 Peres gate. The input vector is I(A,B,C) and output vector is O(P,Q,R) . The output is defined by P=A,Q=AB and R=AB C.
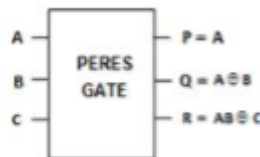

Figure: 4

III. COMBINATIONAL CIRCUITS

Adder and subtractor circuits are basic building blocks of any computing machine. Attempt is made here to realize cost effective reversible half, full adder and subtractors as shown
in figures 5,6,7 and 8 respectively. Further 2:1, multiplexers and 1:4 Demux circuits also realized using reversible gates as shown in figures 20,21,22 and 23..
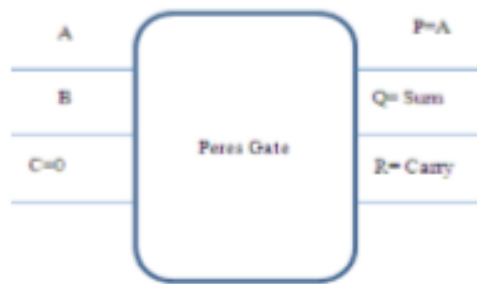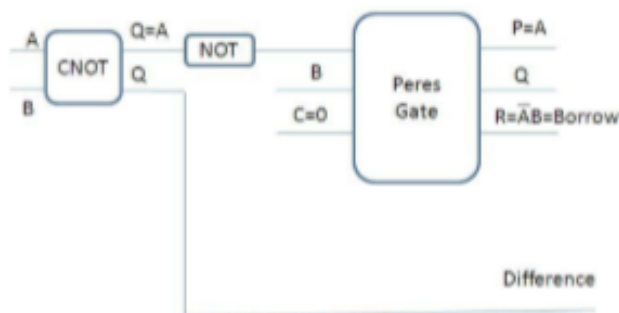
Figure 5: Half Adder

Figure 6: Full Adder

Figure 7: Half subtractor
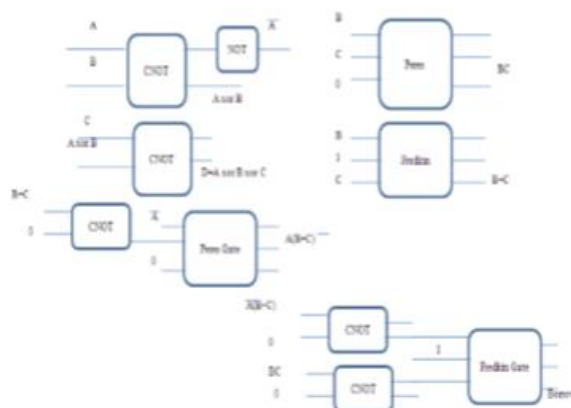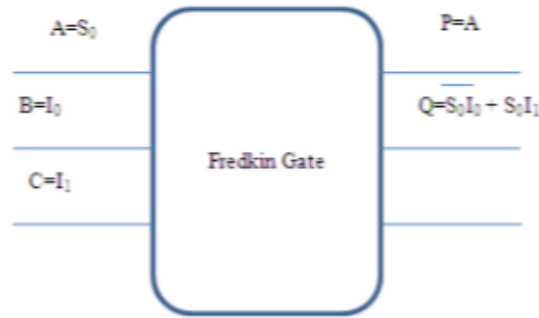

FIGURE 8: FULL SUBTRACTOR
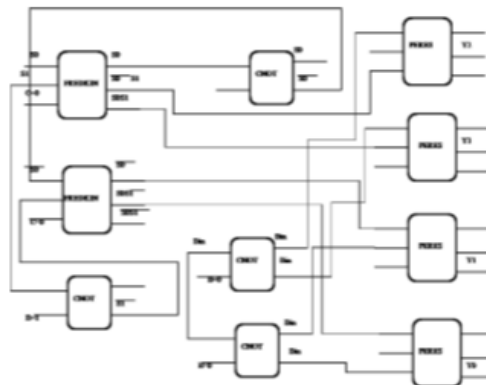
Figure 9:. 2:1 Multiplexer

Figure 10:. 1:4 Demultiplexers

IV.   SEQUENTIAL CIRCUITS:

1.   MASTER-SLAVE D FF WITH ASYNCHRONOUS SET/RESET USING FREDKIN AND FEYNMAN GATES:

The characteristic equation of gated D flip-flop is $Q=CLK'.Q +CLK.D$. The D flip-flop can be realized by one Fredkin gate and one FG. It can be mapped with Fredkin gate by giving CLK, D and Q respectively in 1st, 2nd and 3rd inputs of Fredkin gate . The D FF can be modified as master slave FF. This is further modified with asynchronous Set/Reset as shown in figure 11. In this design the first two Fredkin gates with CLK,D inputs implement the logic for master slave FF. The Fredkin gate used in master latch is the positive enable reversible D Latch, and the Fredkin gate used in Slave latch is the negative enable reversible D Latch .The Fredkin gate with inputs C1, C2 is used to provide the asynchronous set and reset as proposed. The Fredkin gate can be used to avoid the fan out of a signal by assigning that signal to its input A and other two inputs B and C with the inputs B=0 and C=1 as shown in figure12.
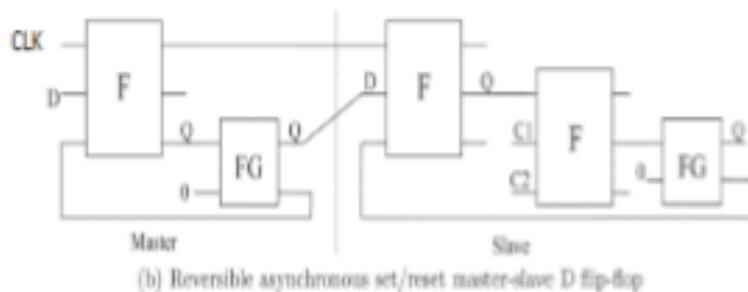

(b) Reversible asynchronous set/reset master-slave D flip-flop

Figure 11

(a) Application of the Fredkin gate to avoid the fanout   (b) Asynchronous reset of the Q and R outputs of the Fredkin gate   (c) Asynchronous set of the Q and R outputs of the Fredkin gate
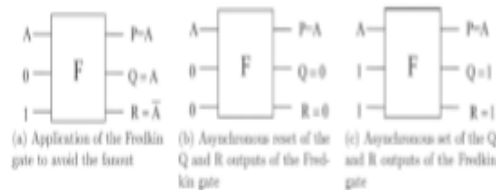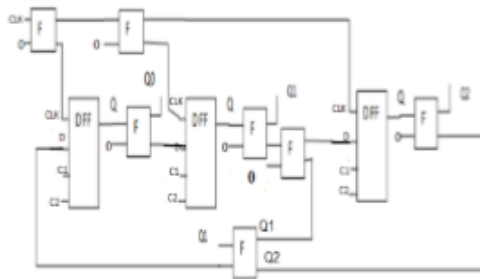
Figure 12

2. DESIGNING LFSR USING REVERSIBLE LOGIC

A linear feedback shift register (LFSR) consists of N registers connected together as a shift register. The input to the shift register comes from XOR of particular bits of the register. On reset, the registers must be initialized to a non-zero value. The LFSR is an example of a maximal length shift register because its output sequence through all 2n-1 combinations (excluding all 0' s).The inputs fed to the XOR are called the tap sequence and are often specified with a characteristic polynomial. We in this paper proposes a design of 3 bit LFSRwith the characteristic polynomial $1+x^2+x^3$. LFSRs are used for high speed counters and Pseudo-random number generators. This pseudo random sequence are handy for built-in self-test and bit error rate testing in communication linksmodules

V.   CONCLUSION

This paper proposes design few combinational circuits like adders, subtractors, mux/demux, encoder using reversible logic. Attempt is made to realize these with minimum quantum cost, garbage outputs and delay so that any complex digital applications can be made more optimized. We have also presented novel designs of reversible D FF with asynchronous set/reset which are optimized in terms of quantum cost, delay and garbage outputs. We conclude that the choice of reversible gates and the design approach to carefully select a reversible gate for implementing a particular logic function will significantly impact the quantum cost, delay and garbage outputs of the reversible design. The application of these FF' s as LFSR is designed and discussed. The application of LFSR as pseudo random bit sequence generator is proposed .Further advancement of the proposed work is to use the proposed D FF' s towards the designs of complex reversible sequential circuits such as FSM.

REFERENCES

[1].   R. Landauer, " Irreversibility and Heat Generation in the Computational Process," IBM Journal of Research and Development, 5, pp. 183-191, 1961.
[2].   C.H. Bennett, " Logical Reversibility of Computation,IBM J.Research and Development,"   pp. 525-532, November 1973.
[3].   Vlatko Vedral, Adriano Bareno and Artur Ekert, " QUANTUM Networks for Elementary Arithmetic Operations," arXiv:quantph/ 9511018 v1, Nov 1995.
[4].   A. Mishchenko, M. Azad Khan, A. Coppola, S.Yanushkevich, " A general decomposition for reversible logic,"   IEEE transactions Proc. RM2001, Starkville, pp: 119-138, 2001
[5].   E. Fredkin and T. Toffoli. Conservative logic. International J. Theor. Physics, 21:219– 253, 1982.