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Weka Hertz Clock Based Weka Bits Per Second P.R.B.S Data Array Encryption A.S.I.C For Parallel Pipelined V.L.I.W Array Based Big Data Distributed Processing /Cloud/Internet Grid Computing Wireless Applications & Products

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----------ABSTRACT----------
The Aim is to Implementation of Weka Hertz Clock P.R.B.S Data Frame Array Encryption Soft H.D.L A.S.I.C I.P Core Architecture Design using Serial to Parallel Data Array Encoder for Parallel Distributed Array Data Computing System based Ultra High Speed Wireless System Software Applications and Products – A.S.I.C Data Serializer-De-Serializer, cloud, cluster, grid, WI-FI,GI-FI Internet computing, 3G,4G,5G Wireless System Software Products and Applications. This Design Architecture contains P.R.B.S Data Frame Registers of 32/64 bit Length, 8 Serial to Parallel Data Encoder Arrays and Weka Clock Frequency Baud Rate Generator /Oscillator and Coding Done by V.H.D.L and Verilog H.D.L Software. Design Implementation Done by Xilinx ISE 9.2i Software I.D.E and Altera Quartus II MODELSIM Simulation Tool. Programming and Debugging Done by Xilinx F.P.G.A Development Kit Xilinx XC 3S 200 TQ 144 F.P.G.A Chip. Design Implementation done through SPARTAN III F.P.G.A.

Keywords: *PRBS – Pseudo Random Binary Sequence, F.P.G.A – Field Programmable Gate Array , A.S.I.C- Application Specific Integrated Circuit. V.H.D.L – Very High Speed Integrated Circuit Hardware Description Language, I.S.E- Integrated Software Environment. I.D.E- Integrated Development Environment*

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I. INTRODUCTION

In Hi-tech Smart Computing Real Time Digital Industrial World & Hi-tech Real time Software Computing World, Every item is smart computing w.r.t speed, power, potential, frequency, Size, performance, Reliability according to Electronic Design and Software Quality Standards. So I've Designed Weka PRBS Data Frame Array Encryption Soft H.D.L A.S.I.C S.O.C I.P Core, using Serial to Parallel Array Encoder. Here I am Implementing Different Patterned Sequences like $2e^{7}$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1, $2e^{48}$-1, $2e^{63}$-1 for High Speed Data Encryption of identification of property of Different PRBS Seed Word Patterns according to Tapping Frequency Standards as per C.C.I.T.T- I.T.U O.150/O.151/O.152 etc. Simply it is one of the Parallel Processing Technique for Randomization of Data from Plain text format to Cipher Text Seed word format. More suitable application are 3G,4G,5G Wireless Mobile and Multimedia ,Consumer Electronic Automation, Medical Diagnostic ,Image & Video Array Processing, Cryptography Automation, Smart Robot Automation, Industrial Automation , Avionics, Automotive Smart WiFi, Internet, Cloud, Cluster, Grid Computing, Super VLIW Parallel Array Distributed Pipe Lined Computing Arrays and Advanced Graphics and Network On Chip Array Cards for MODEMS, Routers. Here the Speed of Weka P.R.B.S Data Frame Array Encryption is in terms of Weka bits per second (Wbps) for all above P.R.B.S Pattern Sequences of different tapping points 7,10,15,23,31 ,48,63 as per Single Data Precision and Double Data Precisions for Big Data Encryption Computing. New Products are all smart Computing Portable Hand Held Digital Automation Applications. This is an Universal IP Core Encrypted Large Automation Data.

Basically The Architecture Contains P.R.B.S – L.F.S.R Data Generator , Weka Clock Frequency Generator, 8 bit Data Encoder Array of different P.R.B.S Data Patten Sequences -$2e^{7}$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1, $2e^{48}$-1, $2e^{63}$-1, etc. P.R.B.S Contains Linear Feedback Shift Register of Different Feedback Tapping points 7,10,15,23,31,48,63 etc. Weka Clock Frequency Generator provide Speed $\mathbf{2^{100}}$ Clock Cycles per second. Simply $\mathbf{2^{50}}$ Clock cycles for Active High Clock Pulse and $\mathbf{2^{50}}$ Clock Cycles for Active low Clock Pulse for processing speed Data Frame Encryption. Estimation Size Of Geometry of P.R.B.S Data Encryption ASIC is In terms of Micro, Nano, and Femto Meters width and Length. The product is mainly suit for Advanced Computing Processors Super V.L.I.W Pipe Lined Distributed Array / Graphics Data Computing Array.

Data Frames Encryption in terms of group of Data Bytes either 4 or 8 Data Bytes width. All the Seed word patterns are processing at an speed of Weka Hertz Clock Frequency Rate outstanding. Speed in terms of Weka Bits per second. This Data Encryption A.S.I.C IP Core suit for all Bus Based Nano /Femto Chip Card Interface Industrial Hardware Card Products / Applications. The Main advantages are more time save and power, reduction of time delays by parallel data encryption technique and high compact and more reliable innovative electronic product. Processing Data is in the form of eye diagrams array. This encryption reduces more bit error rate and A.W.G.N etc.

This Encryption Core Suit Highly Reliable Portable Hand Held Instruments/ Computing products like Mobile Phones, phones, Tablets, Note Book Computers, and eepads. Pen Computers, HiFi Memory Drivers. Large Software Data Compositing Servers, Stations etc. and also Very Suit for Micro/Nano/Femto Boards and Electronic Cards, Graphics Processor Array Cards.

This saves more time and chip complexity, and also more improvement of processing speed of data in terms baud rate Weka Bits per Second for large data computation applications and products like wireless and telecom, data bus communication, Smart consumer electronics, avionics, automotive, image and video, graphics processing, portable multimedia products and applications. This codec is interface with Weka Bytes Memory Shell /SOC for storing large complex data.

II. WEKA HERTZ P.R.B.S DATA FRAME ENCRYPTION A.S.I.C ARCHITECTURE

A. Weka Hertz P.R.B.S Data Frame Array Encryption Soft H.D.L A.S.I.C I.P Core Design Architecture

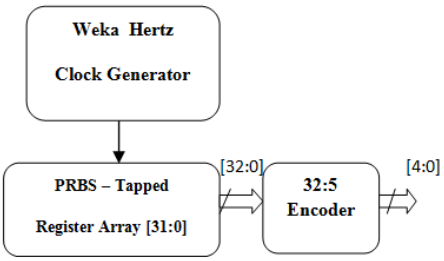
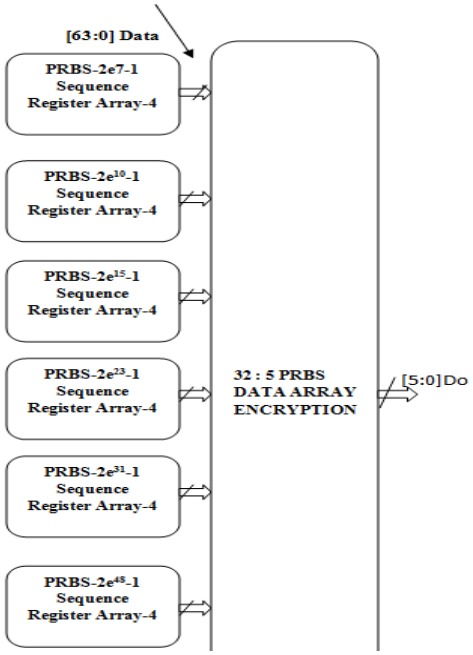


Figure 1.P.R.B.S Tapped Data Frame Array Encryption H.D.L A.S.I.C Architecture

Description: This A.S.I.C I.P Core Consists Weka Hertz Clock Generator , P.R.B.S Tapped Register Arrays of Bit Length 32 Bit Data of Different Tapping Points 7,10,15,23,31,48,63 etc. for Identification and Encryption of Pseudo Random Binary Sequences – $2e^{7}$-1, $2e^{10}$-1,$2e^{15}$-1,$2e^{23}$-1,$2e^{31}$-1,$2e^{48}$-1,$2e^{63}$-1 etc. and 32:5 Priority Encoder for Encryption of PRBS Data Array Sequences of Different Tapping Pattern Sequences as per ITU CCITT Standards.

B. P.R.B.S DATA ARRAY ENCRYPTION DETAILED ARCHITECTURE



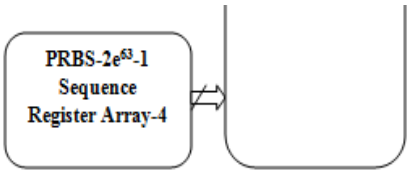


Figure 2. Weka P.R.B.S Data Frame Detailed Architecture

Description: This Design Architecture Seven Different Pattern Registers of Different Tapping Elements - 7,10,15,23,31,48,63 . and This Weka Hertz P.R.B.S Array Consists of Four 7^{th} Tapped P.R.B.S Data Registers ,Four 10^{th} Tapped P.R.B.S Data Encryption Registers , Four 15^{th} Tapped P.R.B.S Data Encryption Registers , Four 23^{rd} Tapped P.R.B.S Data Encryption Register, Four 31^{st} P.R.B.S Data Encryption Register, **all encoded by 32:5 priority Data** Encoder for Identification P.R.B.S Data Frames w.r.t Different Tapping Elements.

III. WEKA P.R.B.S DATA ENCRYPTION DESIGN FLOW REPORTS

A. R.T.L Design Architecture

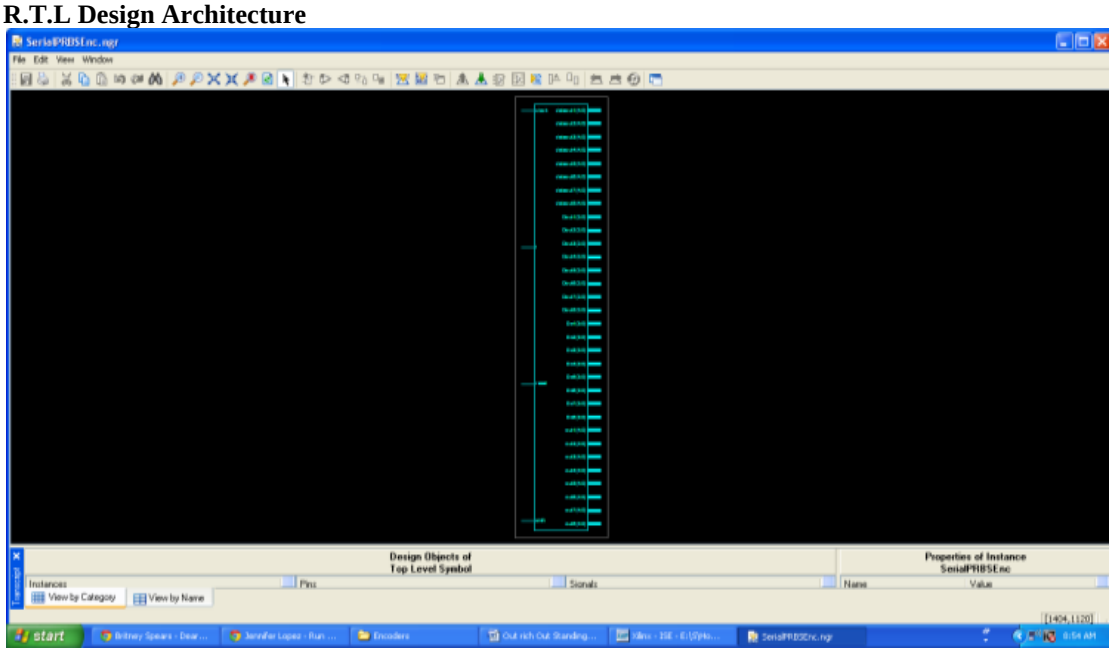
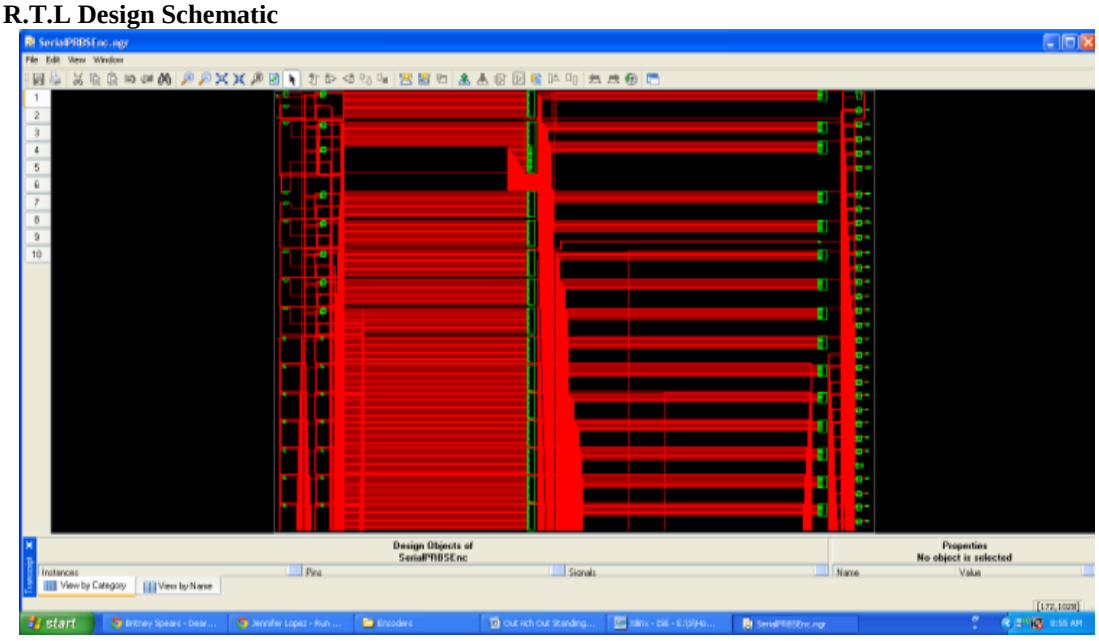
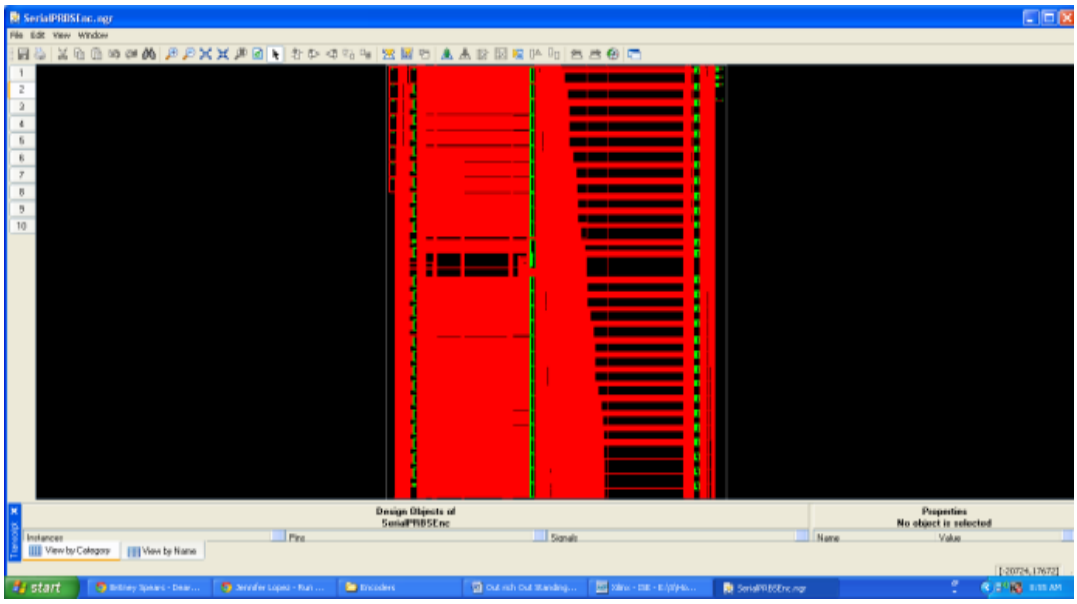
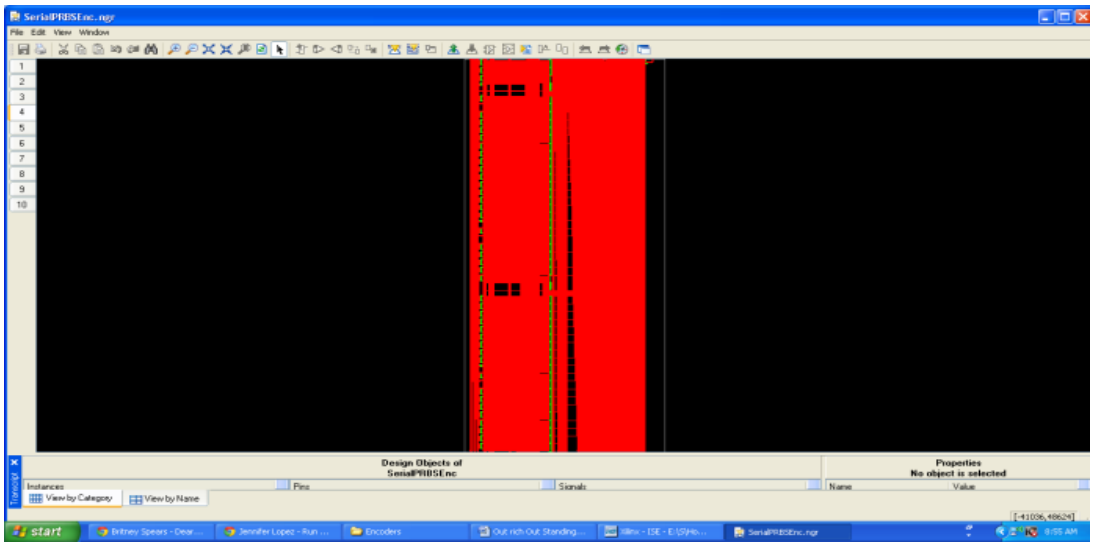


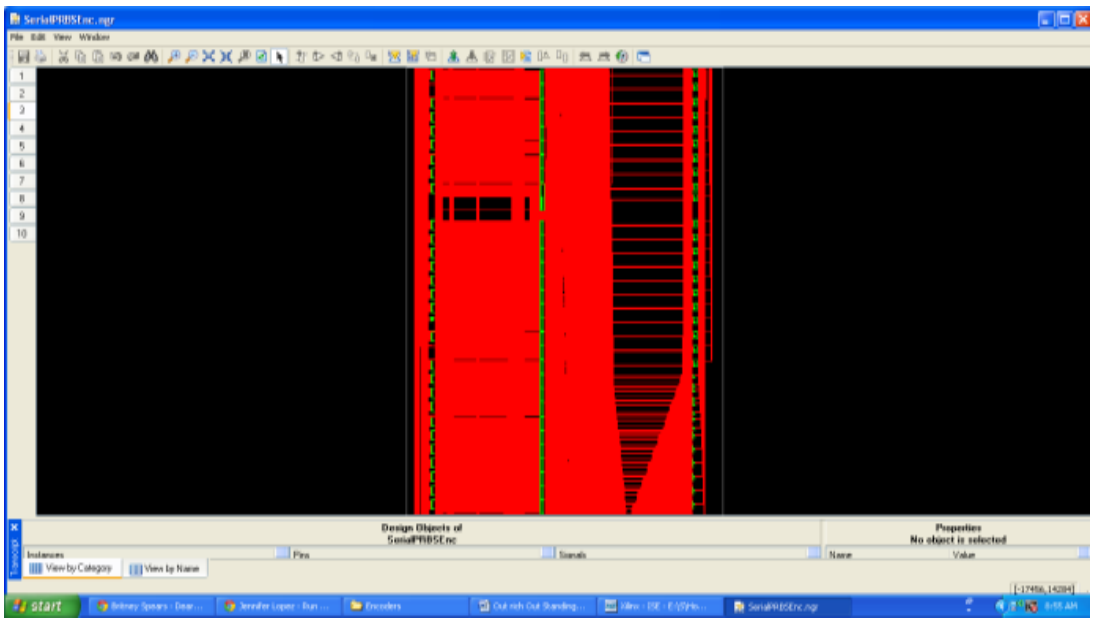
Figure 3. Weka P.R.B.S Data Encryption R.T.L Block

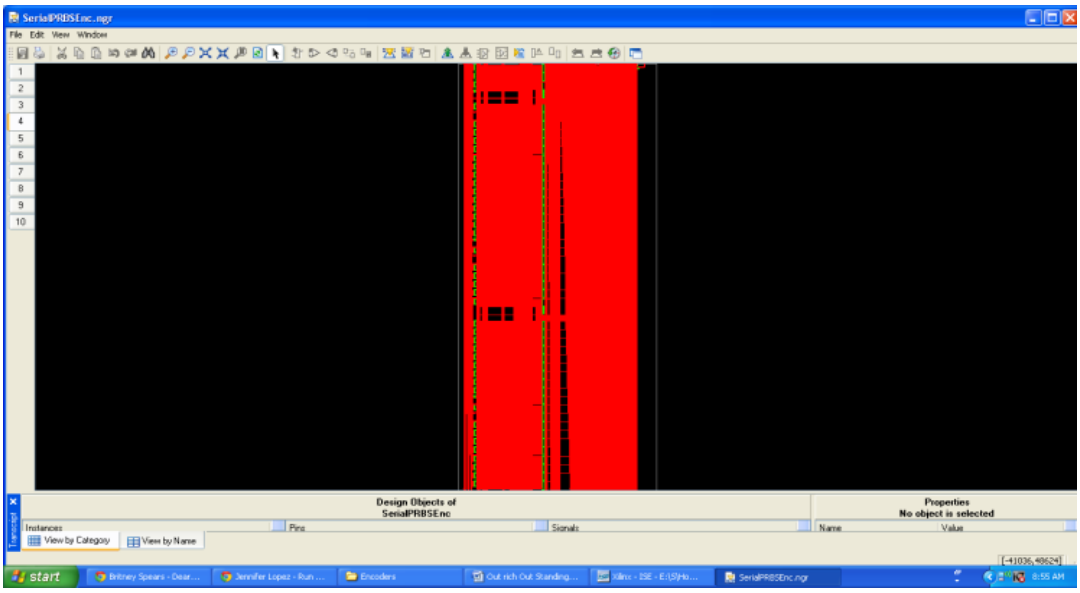
B. R.T.L Design Schematic

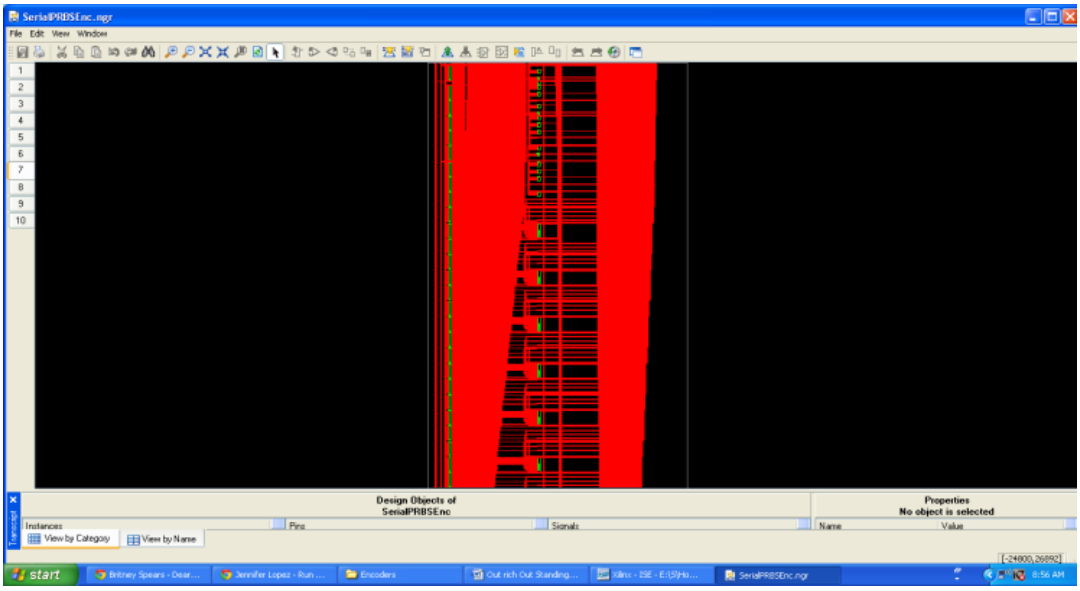


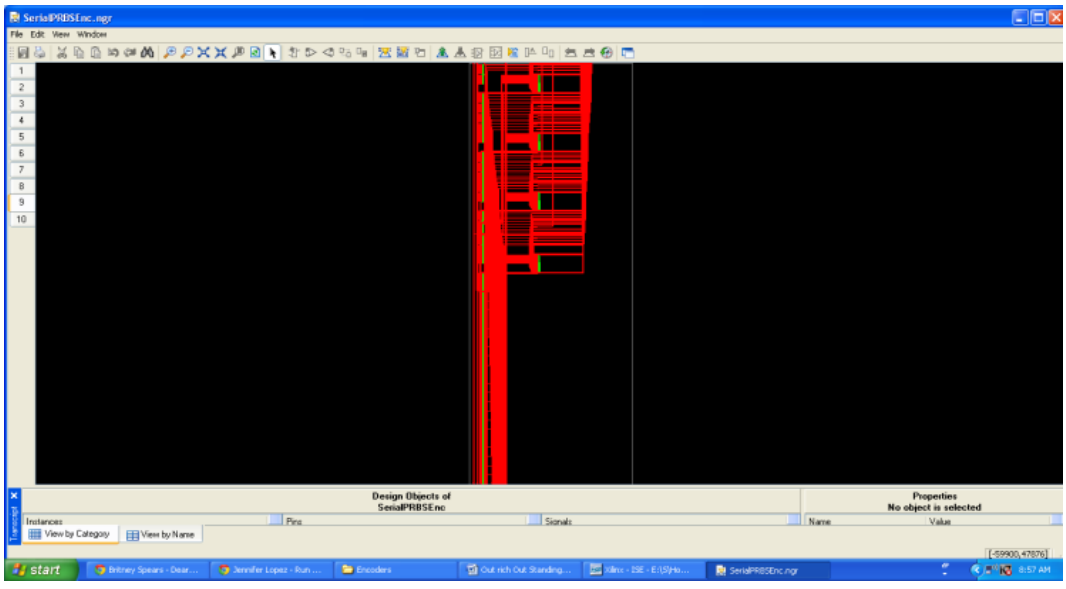












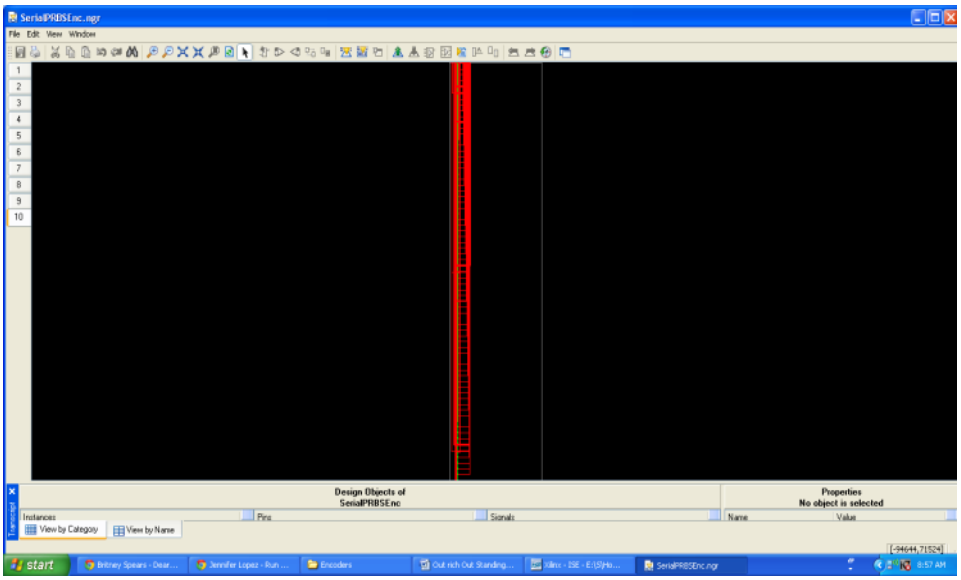
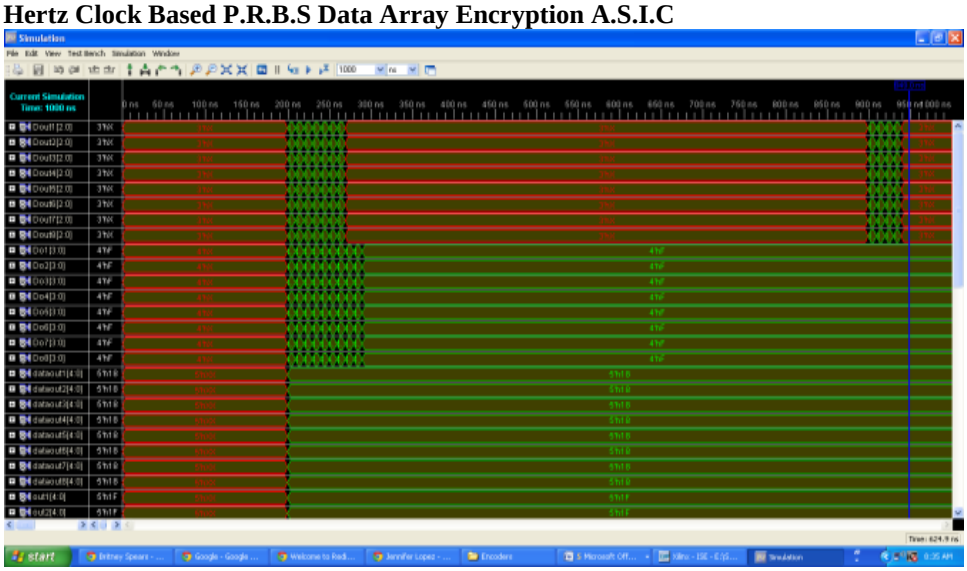
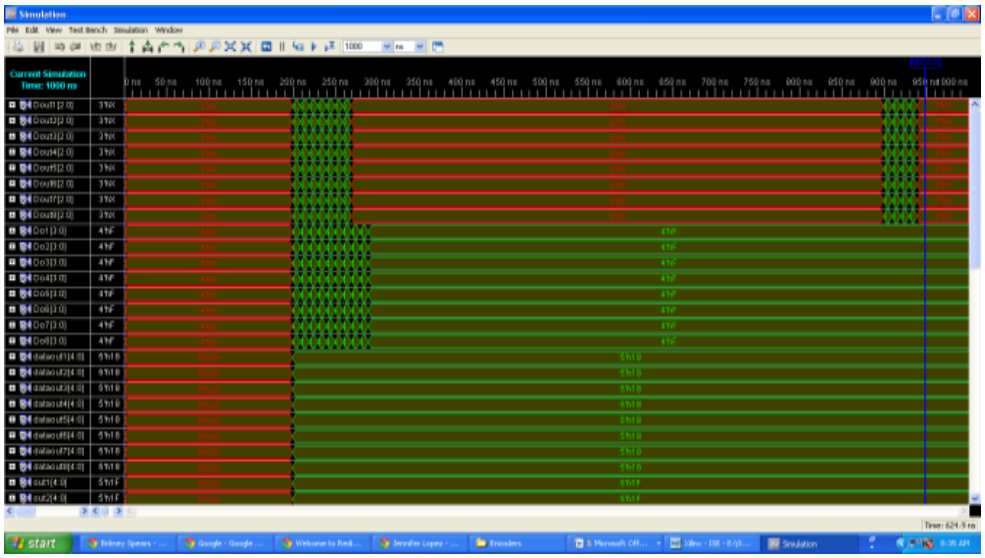


Figure 4. Weka P.R.B.S R.T.L Schematic Design Architecture

IV. SIMULATION WAVE FORM RESULTS

A. Weka Hertz Clock Based P.R.B.S Data Array Encryption A.S.I.C





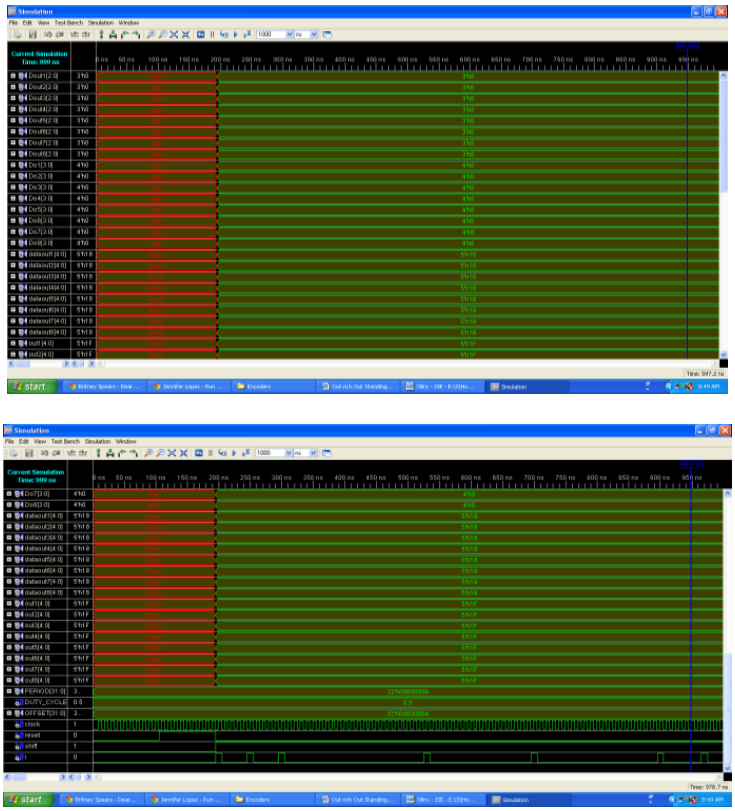


Figure 6. Weka P.R.B.S Simulation Results

V. H.D.L SYNTHESIS REPORTS

HDL SYNTHESIS REPORT
MACRO STATISTICS
 # ADDERS/SUBTRACTORS : 1
100-BIT ADDER : 1
 # COUNTERS : 1
100-BIT UP COUNTER : 1
 # REGISTERS : 65
1-BIT REGISTER : 1
16-BIT REGISTER : 9
24-BIT REGISTER : 8
3-BIT REGISTER : 8
32-BIT REGISTER : 7
4-BIT REGISTER : 8
5-BIT REGISTER : 16
8-BIT REGISTER : 8
 # XORS : 32
1-BIT XOR2 : 15
1-BIT XOR3 : 17
ADVANCED HDL SYNTHESIS REPORT
MACRO STATISTICS
 # ADDERS/SUBTRACTORS : 1
100-BIT ADDER : 1
 # COUNTERS : 1
100-BIT UP COUNTER : 1
 # REGISTERS : 740
FLIP-FLOPS : 740
 # XORS : 31
1-BIT XOR2 : 15
1-BIT XOR3 : 16

VI. VLSI – IC SOFTWARE DESIGN FLOW CHART

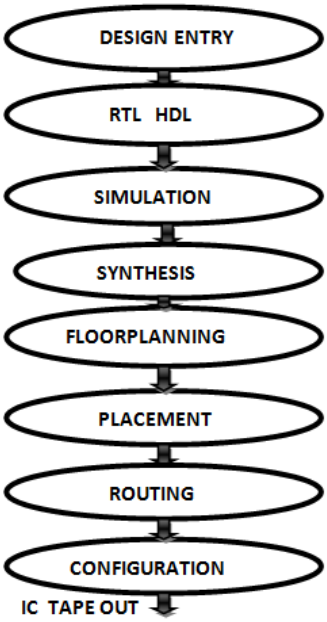


Figure 7. VLSI IC- EDA Software Design Flow Chart

VII. CONCLUSION

Designed **Weka PRBS** for Ultra High Speed Wireless Communications, This Design is mainly intended for Ultra Very High Long Distance Communication at the frequency rate of Weka Bits per Second. And this product is very suited for All Very Advanced Smart Digital Computing Communication Products like Advanced 3G,4G,5G,6G, Hi-Fi Space Communication ,Satellite Communication Products. DESIGNED WEKA PRBS DATA ENCRYPTION ASIC IP CORE FOR HIGH SPEED PARALLEL VLIW -DATA COMPUTING / CLOUD COMPUTING/CLUSTER COMPUTING PRODUCTS

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