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Ultra High Multi Clock Frequency Spectrum -Zetta,Yotta,Xona, Weka Hertz Real Time Clock P.R.B.S Data Framer Array A.S.I.C I.P Core Encryption And Decryption Of Different Patterns For Large/ Big Wireless Data /Cloud/Cluster /Parallel Distributed Computing Stations

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----------ABSTRACT----------
The Aim is to Design and Implement the Ultra High Speed Multi Clock Frequency Spectrum – Tera, Peta, Exa, Zetta, Yotta, Xona , and Weka Hertz Clock P.R.B.S Data Framer Encryption and Decryption Array A.S.I.C S.O.C I.P Core of Different Tapped Seed Word Pattern Sequences - $2e^{7-1}$, $2e^{10-1}$, $2e^{15-1}$,$2e^{23-1,}$ $2e^{31-1}$, $2e^{48-1}$, $2e^{52-1}$, $2e^{63-1}$, $2e^{127-1}$, $2e^{255-1}$ etc for Large /Big Wireless Data /Cloud/Cluster/Parallel Distributed Computing Stations of Different Data Bytes Storage Capacity – Mega, Giga,Tera,Peta,Exa,Zetta,Yotta,Xona,Weka,Vendica Bits/Bytes Per Second and Data Length in terms of Frames,SuperFrames,Very long word ,Super Very Long Word, large array randomized data packets and words for parallel Distributed Computing Data Processing and Storage, execution o f Internet data packets , Cloud /Cluster Data Computing Stations. Implementation Done By soft HDL Procedures – Verilog H.D.L and V.H.D.L & Debugging Done By F.P.G.A –Xilinx 3s4000lfg900-4.

Keywords: *A.S.I.C- Application Specific Integrated Circuit, S.O.C- System On Chip , IP – Intellectual Property Core, F.P.G.A – Field Programmable Gate Array, P.R.B.S- Pseudo Random Binary Sequence, L.F.S.R-Linear Feedback Shift Register, V.H.D.L –Very High Speed Integrated Circuit Hardware Description Language, C.C.I.T.T-(I.T.U)-Consulting Committee for International Telegraph and Telephone, I.T.U – International Telecom Union.*

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I. INTRODUCTION

The Pseudo Random Data Framer Array Encryption and Decryption is mainly used for Encrypted and Decrypted the Randomized Data for all wireless and telecom, cryptographic Data Security and Data Communication and Networking Protocol Computing applications and products. The main aim of the design is to Pseudo Random binary Sequence Pattern Serial and Parallel Data Encryption and Decryption for identification of Property of Pseudo Random binary Sequence SEED WORD Patterns – $2e^{7-1}$, $2e^{10-1}$, $2e^{15-1}$,$2e^{23-1,}$ $2e^{31-1}$, $2e^{48-1}$, $2e^{52-1}$, $2e^{63-1}$, $2e^{127-1}$, $2e^{255-1}$ etc as per Single Precision and Double, Quad Data, Octal Data Array Precision Highly Stringent Data Standards of Different High Speed Data w.r.t ultra High Clock Frequencies Synchronization- Mega , Giga , Tera, Peta, Exa, Zetta, Yotta, Xona , Weka , Vendica Hertz and also Data Speed in terms of Data Bytes, Frames, Super Frames, Very Long word Frames, Super Very long Word Frames, Data Packets, Internet Data Packets and Baud Rate in terms Mega , Giga , Tera, Peta , Exa, Zetta, Yotta, Xona , Weka , Vendica Bits/ Bytes per Second and PRBS Data Encryption and Decryption Memories are in terms of Mega, Giga, Tera, Peta, Exa , Zetta, Yotta, Bronto , Geop Bytes, Frames , Super Frames , Very long Super Word Frames, large array randomized data packets and words for parallel Distributed Computing Data Processing and Storage, execution o f Internet data packets , Cloud /Cluster Data Computing Processing and storage ,execution purpose. All these different groups of P.R.B.S L.F.S.R Frame Array Registers $10e^{7}$-1,$10e^{10}$-1,$10e^{15}$-1,$10e^{31}$-1,$10e^{48}$-1,$10e^{52}$-1,$10e^{63}$-1, $10e^{127}$-1, $10e^{255}$-1 Frame array groups with different process tapping elements (7,6),(10,7),(14,15),(28,31)(42,47),(48,51),(57,63),(123,127)(247,255) are processed in the form of parallel and independently for improvement of speed and performance, reduction of very less time delay and complexity of the design. The Intention is for Hi-Fi Industrial Standard P.R.B.S **Data Framer Array A.S.I.C S.O.C Soft I.P** Core Design as per C.C.I.T.T-I.T.U O.150/O.151/O.152/O.153 Software Industry Standards, and Software Design implementation using V.H.D.L & Verilog H.D.L Coding, Programming and

Debugging done using F.P.G.A –Xilinx 3s4000lfg900-4 . This A.S.I.C is mainly used for processing Parallel Pipelined Distributed Array Data Computing /Cloud Computing for Large High Speed Long Distance Wireless Communication Data Computing Products (Long Terminal Equipment –A.S.I.C) like Cloud Data Computing Wireless Network Stations/Shells, Advanced Distributed Processor Array Computing Products / Applications like 3G, 4G, 5G, 6th sense Processing and Computing. Of large big data.

In Hi-tech Smart Digital Computing Software World, So many advanced smart wireless, consumer mobile and internet cloud computing on chip based products and Parallel Distributed Processor Array based Computing Products came to the market like advanced eepads, notepads, tablets, iphones, Pocket Mobile Multimedia Computer, GPS Mobile Computer, Parallel Pipelined Array Based Distributed Computing Based Processors and Graphics Processors, Smart wireless network on chips ,WiFi,GiFi,WiMAx, and system on chip based wireless products , advanced portable handheld electronic instrument products, because of high speed wireless data packets processing and computing, transmission and reception in terms of Giga bits per second (Gbps) baud rate synchronizing with clock and time. According Current Market Trends , I Designed P.R.B.S Framer Array A.S.I.C SOC Soft I.P Core Designed for High Speed Computation in terms of Tera / Peta / Exa / Zetta /Yotta/Xona/Weka Hertz frequency baud rate(bits per Second) based wireless ,consumer, Medical, Image and Video Processing, avionics, space communication based High Speed Data Computation purpose. In Hi-tech Smart Computing Real Time Digital Industrial World & Hi-tech Real time Software Computing World, Every item is smart computing w.r.t speed, power, potential, frequency, Size, performance, Reliability according to Electronic Design and Software Quality Standards.

The Pseudo Random Binary Sequence Array A.S.I.C consists of 32 P.R.B.S Registers out of 32 Registers PRBS LFSR Registers- $2e^{7}$-1, $2e^{10}$-1, $2e^{15}$-1 , $2e^{18}$-1,$2e^{23}$-1, $2e^{31}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 of each Four Register Array, Each of the Four Register form Frame Array Group, The Multiple P.R.B.S Framer Array A.S.I.C Products Integrated to form multiple framer arrays of Different P.R.B.S L.F.S.R Registers with Different Tapping Elements 8,16,32,64,128,256 Bit of Different Random Pattern Sequences $2e^{7}$-1,$2e^{10}$-1,$2e^{15}$-1,$2e^{31}$-1,$2e^{63}$-1,$2e^{127}$-1, $2e^{255}$-1 with tapping point (7,6),(10,7),(14,15),(28,31)(42,47),(48,51),(57,63),(123,127)(247,255) of different data frame arrays and lengths. P.R.B.S A.S.I.C S.O.C processing multiple array of frames of data at a time processed and computing by implementation parallel distributed pipelined array computing technique for data fetching and decoding and executing large data frames for particular application/product This is an single chip Universal ASIC S.O.C Solution for all products and applications like wireless and telecom, bus data communication and networking, cloud and internet computing, super Grid/Cluster/Parallel Distributed computing solutions, consumer and mobile smart digital electronics, satellite and space, aerospace engineering, automotive applications and products.

I' Designed and Implemented the product for parallel Distributed Array Processor Computing based Products and Applications for Transmission and Reception and Processing of Data in High Speed Computing in the form of P.R.B.S Data Packets and Frames. The main intension the design is for Highly Reliable w.r.t complexity, performance and size and power consumption. At a time process the 8 x 4 Frames of data processing and computing by synchronizing with single clock pulse w.r.t different High Data Frequency Clock Rates in terms of Tera, Peta, Exa, Zetta, Yotta,Xona,Weka Baud Rates. This P.R.B.S Framer Array A.S.I.C is very suit for all universal processing products and applications Specific to Parallel Distributed Pipe lined Array Processing Computers for processing and computing the instruction and data fetching , decoding , executing randomly in repeated number of times according to tapping processing elements at very high frequency rates in terms of Tera , Peta, Exa , Zetta , Yotta, Xona ,Weka Hertz Clock Frequency Baud Rates. This P.R.B.S Framer Array A.S.I.C is for computing and processing the large Complex Cloud data computing in the form of Frame Arrays 32 frames at a time for large computational data based applications and products at very high frequency baud rates – Tera, Peta, Exa, Zetta, Xona, Yotta, Weka Hertz Clock Frequency. Also the P.R.B.S Framer is for processing and computing the Large Image , Video , Graphics , Medical Diagnostic Images and products at a very high speed w.r.t baud rate speed in terms of above mentioned frequencies by synchronizing with Single Clock. The PRBS Framer Array Processing the Large Data Frames for Hi-Fi Electronic Design Automation products Avionics as per D.O-178 Software standards, Automotive as per I.E.C-50128/9,60128 C.E.N.L.E.C Standards.

I' Implemented the P.R.B.S Framer Array A.S.I.C S.O.C Design using Parallel Distributed Pipeline Array Computing Technique for fetching , decoding, executing all random data frame arrays. these random seed word frames processed in the form of parallel groups, the advantages are save more number of data frame array packets , reduction of multiple IO Ports , and number of Data shift Registers , improvement of Processing speed, all these data seed words are repeated number of times w.r.t data width. For example $10e^{7}$-1 PRBS – LFSR Register, the length of randomized data width is 2^{L}-1. Similarly other PRBS Random Pattern Sequences $10e^{10}$-1,$10e^{15}$-1,$10e^{31}$-1 of different tapping elements. The product is very suit for processing large data packets in the internet data computing and cloud computing, processing speed is very high and also this product is very suit for reduction of internet data packets frame array traffic errors and reduction of noise , eliminating internet data

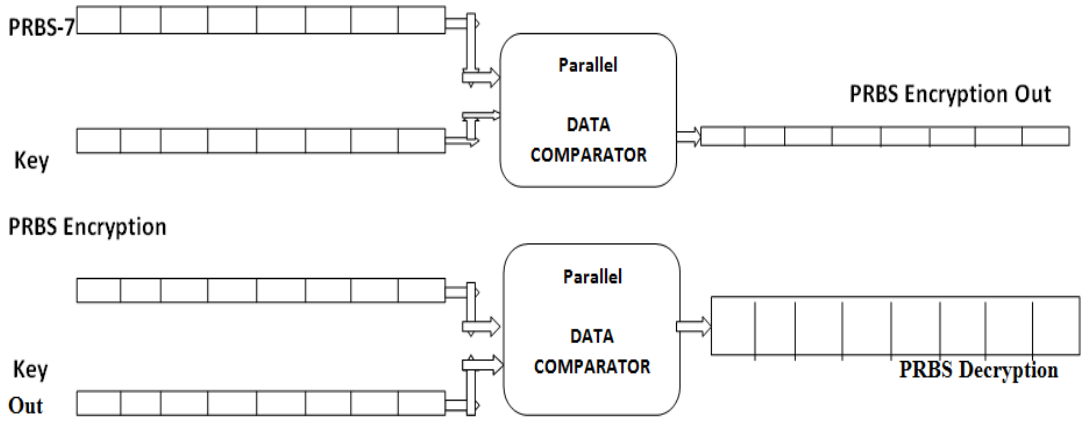
packets traffic loss. This saves more processing time delay , reduction of more hardware complexity and size on the cards/boards due to this S.O.C. This product is also very suit for processing and computing large data frames at a time without any data loss in cloud computing and network racks and stations ,server arrays. This reduces more processing delay time, easy debug process, flexible and compatible, more reliable of real time data computing. Switching of data frames is so easy , because of I developed parallel processing and computing data technique. This product is operated with different clock frequencies – Tera, Peta, Exa, Zetta, Yotta, Xona, and Weka Hertz Clock Frequency Baud Rates for very high speed processing . Instead of using multiple PRBS Transceivers , I Implemented in the single P.R.B.S Framer Array A.S.I.C S.O.C IP Core. And this product mainly intended for very high long distance communication purpose. For avoidance of traffic data collision and loss of data packets, also for clean digital data without unwanted spikes / noise occurred while doing transmission and reception, I used Parallel Distributed P.R.B.S Framer Array A.S.I.C IP Core.

This product is not only suit for Cloud and internet data computing E.D.A applications/products, this P.R.B.S Framer A.S.I.C Array also suit for various electronic applications/products like Graphics Processing and Animation, Image and Video data Processing (Digital Cameras) , Cryptography applications, S.O.C Design data Testing by processing of Random Array Data Frames, Smart Real time Digital Consumer Mobile and Multimedia Electronic Data Processing, large wireless and telecom data communication engineering applications and also for space,satellite,aerospace,automotive data processing products and applications. In Image processing, all the pixel data array frames data processed in the form of data frame windows by using PRBS Framer Array A.S.I.C. Very less time takes to scan the window frames in the form of vertical and horizontal lines and frames format. In SOC Testers also this product dominates lot compared to other testing techniques like Boundary Scan Array S.O.C, Logic B.I.S.T and B.I.L.B.O Arrays. Testing Speed is so very high and also at a time scanning and testing multiple large data frame arrays using the product, simply this product test multiple S.O.C's at a time. This product also very suit for Very High Advanced High Speed Serial and parallel Data Communication Protocols – R.S 232,485,U.A.R.T ,U.S.B 2.0,3.0,P.C.I,S.A.T.A Frame Arrays processing and Computing while transmission and reception of long distance communication protocol applications and products. Also this product is very suit for processing data in Network on Chip Computing based Wi-Fi router ASIC products. Not only communication applications , this product is very suit for Aerospace and satellite vehicles for processing and computing large data frames in the form of parallel computing without any data loss and miniature catastrophic data failures and very less noise. This product is very highly reliable and complete Quality soft A.S.I.C IP Core Product.

II. P.R.B.S DATA FRAMER ARRAY, ENCRYPTION AND DECRYPTION DESIGN ARCHITECTURES

P.R.B.S Data Encryption & Decryption Diagram of different P.R.B.S Patterns

Logic Design Architecture – Serial and Parallel PRBS Data Encryption and Decryption Design Architecture



This A.S.I.C Soft I.P Core Design Module of P.R.B.S Data Encryption and Decryption basically consists multiple P.R.B.S Designs of different Pattern sequence lengths $-2e^{7-1}$, $2e^{10-1}$, $2e^{15-1}$,$2e^{23-1,}$ $2e^{31-1}$, $2e^{48-1}$, $2e^{52-1}$, $2e^{63-1}$,$2e^{127}-1$,$2e^{255}-1$ are processed randomized Data frequencies and numbers are in parallel for advanced Digital Smart Parallel Distributed Computing A.S.I.C and Internet, Cloud/cluster Soft IP Core computing products and applications in advanced Data Communication and Networking Protocol soft I.P Cores /Cards and Serializer and Deserializers, Data interface Cards, Advanced A.S.I.C and F.P.G.A Application Cards/Boards or S.O.C Designs and Secure Data Communication and Cryptography Applications . etc Due to

this we can easily interface data randomly w.r.t data design cards of different length of bits and Different speed rate in terms of Data bytes, words, frames, super frames, super word frames, packets etc.

III. PRBS DATA FRAMER ARRAY ENCRYPTION KEY

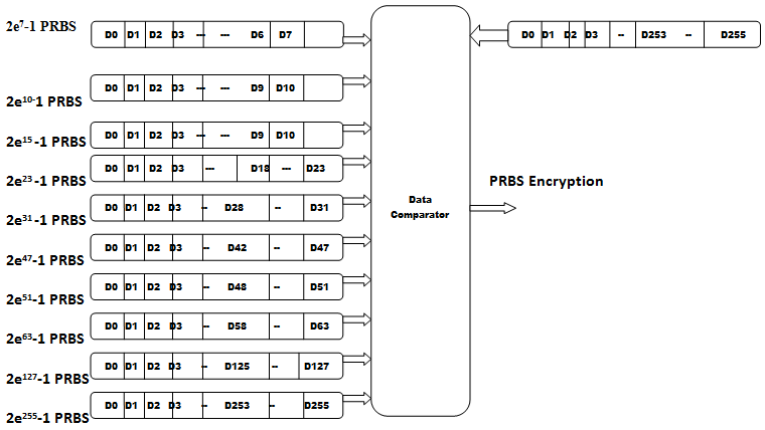


Fig 1.0 PRBS Data Framer Array Encryption

A. PRBS Data Framer Array Decryption

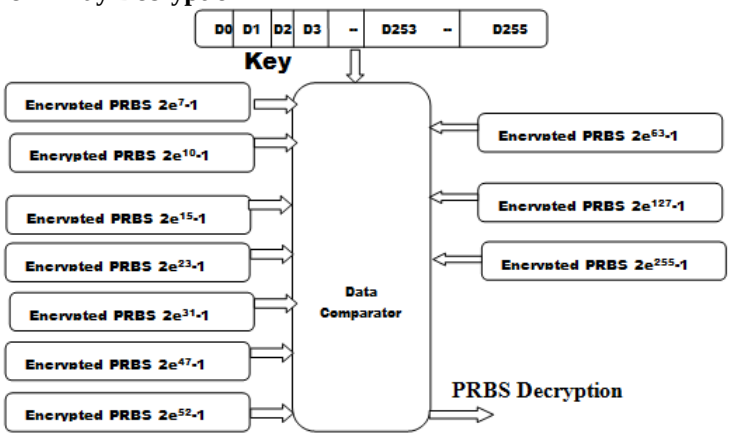


Fig 1.1 PRBS Data Framer Array Decryption

B. P.R.B.S Framer Array ASIC S.O.C Architecture

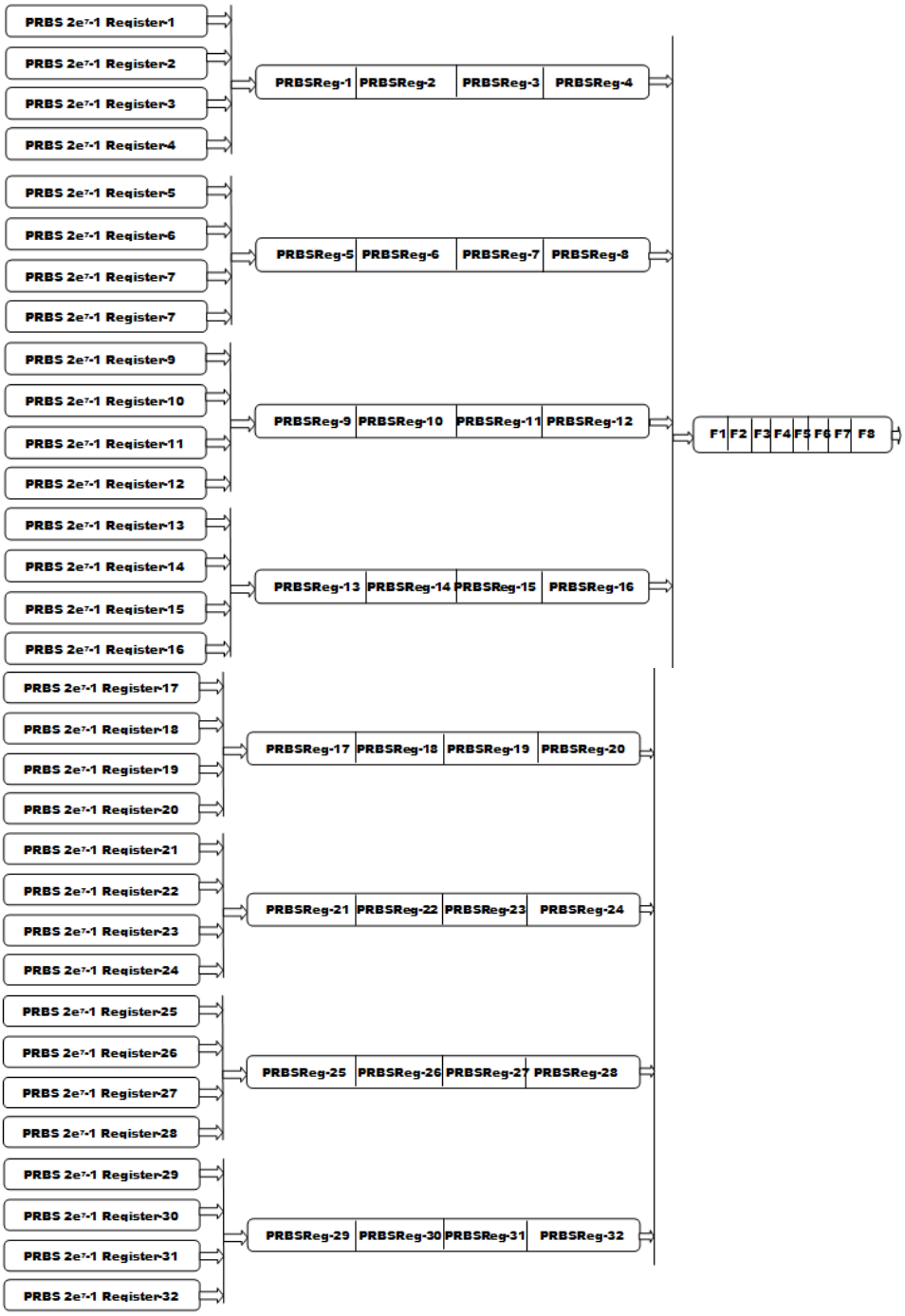


Fig.1.2. P.R.B.S FRAMER ARRAY ASIC of Tapped Pattern Sequences
-$2e^{7}$-1, $2e^{10}$-1, $2e^{15}$-1 , $2e^{18}$-1,$2e^{23}$-1, $2e^{31}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1

C. Description

The Pseudo Random Binary Sequence Array ASIC consists of 32 PRBS Registers out of 32 Registers PRBS LFSR Registers- $2e^{7}$-1, $2e^{10}$-1, $2e^{15}$-1 , $2e^{18}$-1,$2e^{23}$-1, $2e^{31}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 of each Four Register Array, Each of the Four Register form Frame Array Group, The Multiple P.R.B.S Framer Array A.S.I.C Products Integrated to form multiple framer arrays of Different P.R.B.S L.F.S.R Registers with Different Tapping Elements 8,16,32,64,128,256 Bit of Different Random Pattern Sequences $2e^{7}$-1,$2e^{10}$-1,$2e^{15}$-1,$2e^{31}$-1,$2e^{63}$-1,$2e^{127}$-1, $2e^{255}$-1 with tapping points (7,6) ,(10,7),(14,15),(28,31),(58,63),(126,127),(253,255) of different data frame arrays and lengths. P.R.B.S A.S.I.C S.O.C processing multiple array of frames of data at a time processed and computing by implementation parallel distributed pipelined array computing technique for data fetching and decoding and executing large data frames for particular application/product This is an single chip Universal ASIC S.O.C Solution for all products and applications like wireless and telecom, bus data communication and

networking, cloud and internet computing, super Grid/Cluster/Parallel Distributed computing solutions, consumer and mobile smart digital electronics, satellite and space, aerospace engineering, automotive applications and products.

D. Universal P.R.B.S Super Frame Array ASIC S.O.C Design Architecture

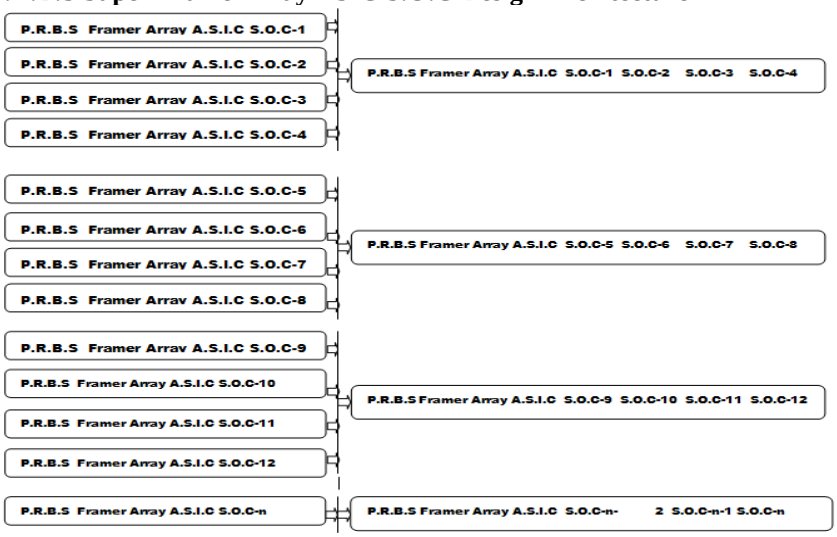


Fig.1.3. P.R.B.S FRAMER ARRAY ASIC

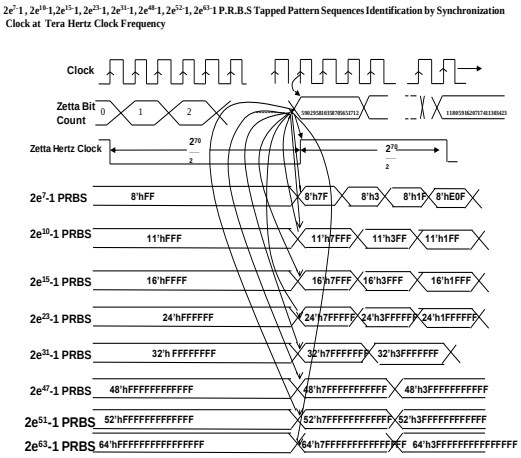
E. Description

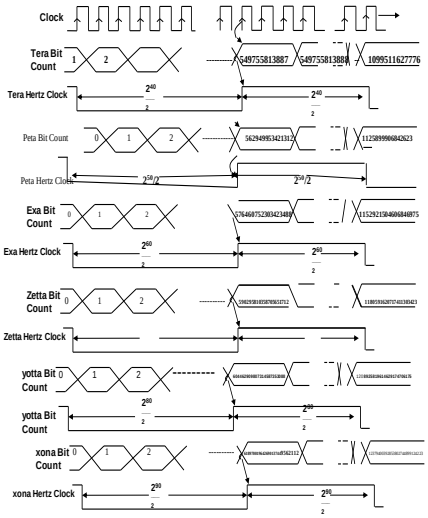
The Above Architecture Consists P.R.B.S Framer Array A.S.I.C S.O.C 1,2,3,4 ----- 10,12,13,14 , ----n-3,n-2,n-1,n are grouped and divided in to P.R.B.S Framer Array A.S.I.C S.O.C Very long word Super Frame Array packets Format. All integrated form multiple very long word super frame array packets A.S.I.C S.O.C Architecture. All such super frames again grouped and integrated to form very long word super frame array A.S.I.C S.O.C Architectures for processing and computing multiple Cloud Array and Internet array computing solutions using these products. All the very long word super framer array data packets processed in the form of parallel pipelined array computing ,for large computing data applications, at a very high speed and long distance communication purpose, For high speed I am using Giga, Tera ,Peta , Exa, Zetta, Xona, Weka, Vendica, 2^{1000}, etc Super frame carrier synchronous Clock frequencies with accurate data communication without any data packets loss and internet traffic loss, this product is very futuristic and even this engineering soft IP Core product is not available in the world market, may be hundreds of years time takes this product will come to the market in the major fortune, now I designed with highly intelligence logic design implemented through software code.

IV. FORMULAS – PSEUDO RANDOM BINARY SEQUENCE POLYNOMIALS

PRBS $2e^{7}-1 = 1 + x^{6}+ x^{7}$
PRBS $2e^{10}-1 = 1 + x^{3}+ x^{10}$ (2)
PRBS $2e^{15}-1 = 1 + x^{14}+ x^{15}$ (3)
PRBS $2e^{23}-1 = 1 + x^{18}+ x^{23}$ (4)
PRBS $2e^{31}-1 = 1 + x^{28}+ x^{31}$ (5)
PRBS $2e^{47}-1 = 1 + x^{42}+ x^{47}$ (6)
PRBS $2e^{51}-1 = 1 + x^{48}+ x^{51}$ (7)
PRBS $2e^{63}-1 = 1 + x^{58}+ x^{63}$ (8)
PRBS $2e^{127}-1 = 1 + x^{123}+ x^{127}$ (9)
PRBS $2e^{255}-1 = 1 + x^{247}+ x^{255}$ (10)

V. CLOCK SYNCHRONIZATION WAVE FORM DIAGRAMS





VI. P.R.B.S TELECOM FREQUENCY STANDARD TABLE

PRBS TYPE	STANDARD	SUGGESTED DATA RATE (Kilo Bits Per Second)	FEED BACK TAP
$2e^{7}$-1	ITU-T O.150	14.4	7,6
$2e^{10}$-1	ITU-T O.150	64	10,3
$2e^{15}$-1	ITU-T O.151	1544, 2048, 6312, 8448, 32064, 44736	14,15
$2e^{23}$-1	ITU-T O.150	34368, 44736, 139264	18,23
$2e^{31}$-1	ITU-T O.150	1.2,1.5 G .b.p.s	28,31
$2e^{48}$-1	ITU-T O.150/151/152	500 G.b.p.s	48,42
$2e^{52}$-1	ITU-T O.150/151/152	1 T.b.p.s	52,47
$2e^{63}$-1	ITU-T O.150/151/152/153	500 T.b.p.s	48,63
$2e^{127}$-1	ITU-T O.150/151/152/153	1 P.b.p.s	123,127
$2e^{255}$-1		500 P.b.ps and 1 E.b.p.s	247,255

Table.1. PRBS Pattern Sequences as per ITU O.150/O.151/O.152 Standards

VII. VLSI – IC F.P.G.A SOFTWARE I.P CORE – P.R.B.S FRAMER ARRAY A.S.I.C. S.O.C DESIGN FLOW CHART

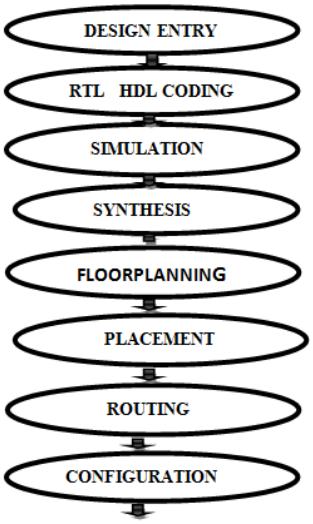


Fig1.4: VLSI IC EDA Software Design Flow

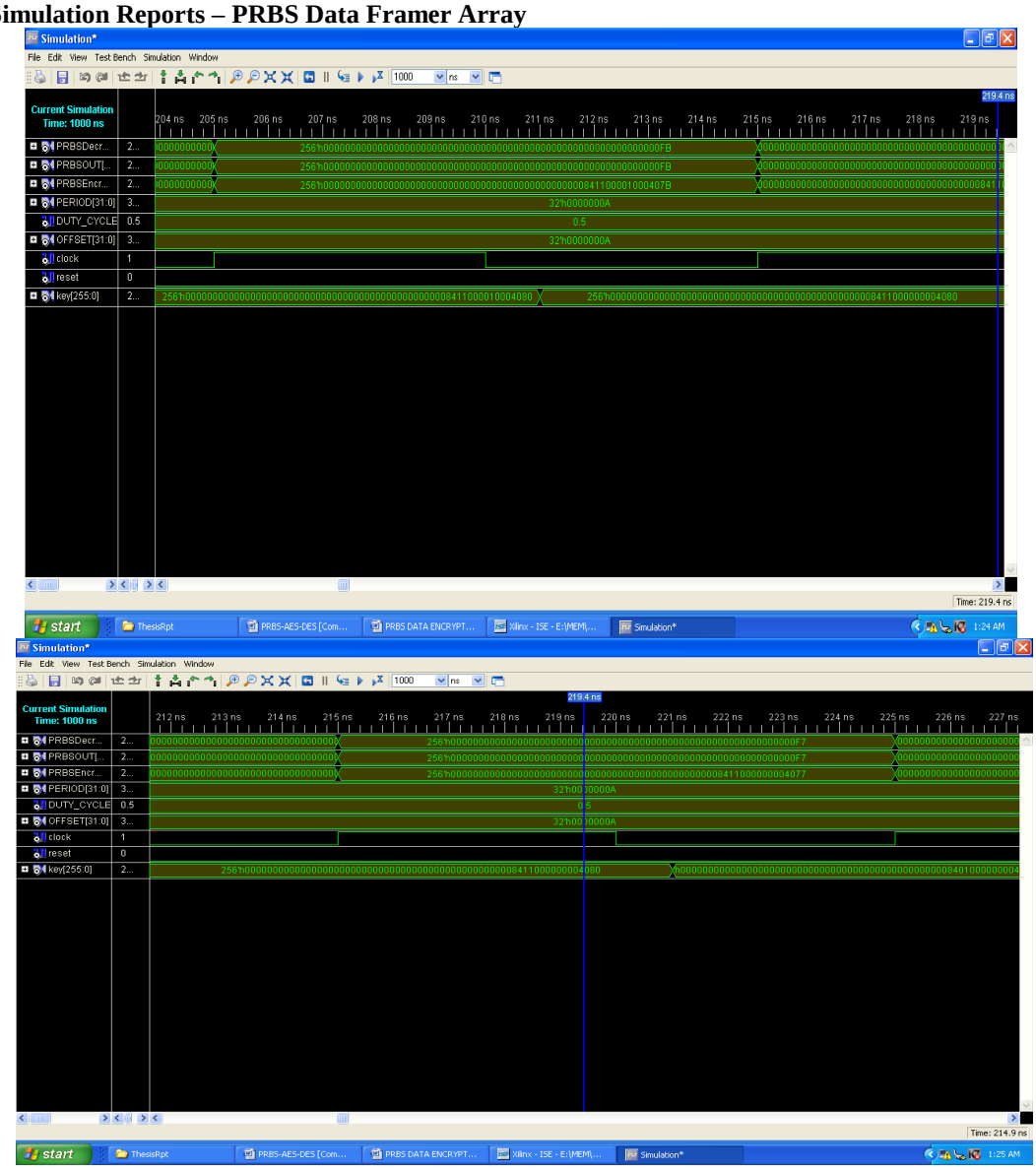
7.1.1 Description

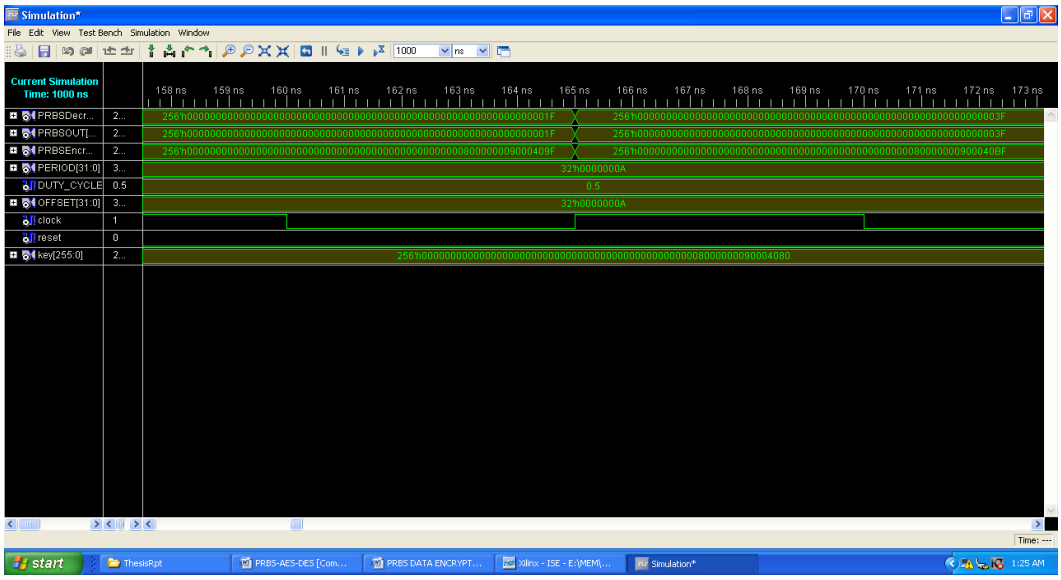
This is Standard Industry Design Flow Chart for Delivery of VLSI IC Chip Design Soft IP Core Products/Designs. Initially entering RTL Design of P.R.B.S Framer A.S.I.C S.O.C I.P Core through Design Entry Step, After That RTL VHDL & / Verilog HDL Coding Done through HDL RTL Design Software Editor of both behavioral and Data flow models using Xilinx ISE Software . Verification & Running the Functionality of RTL HDL Design Description through by Simulation and Abstract the Description in to Gate Level Net list

using Synthesis, subsequently Place & Routing through FPGA Placed Design & Router and Programming and Debugging Done through Reconfiguration using JTAG Debugger. All the Design flow reports generated by using Xilinx ISE 10.1i ISE Software Design Tool. This Design Flow Estimates the number of Placed Design Blocks and Routing Paths (Number of Routing Wires connected on F.P.G.A). This Xilinx ISE FPGA Design Flow not only estimates placed and routed design components on FPGA, also estimates number of clocks, static timing, power ,performance , speed, mapping before and after, pre and post simulation and synthesis, Floor planning of hardware P.R.B.S. Framer Array A.S.I.C S.O.C I.P Core etc.

VIII. FPGA INDUSTRIAL DESIGN FLOW REPORTS

8.1.1 Simulation Reports – PRBS Data Framer Array

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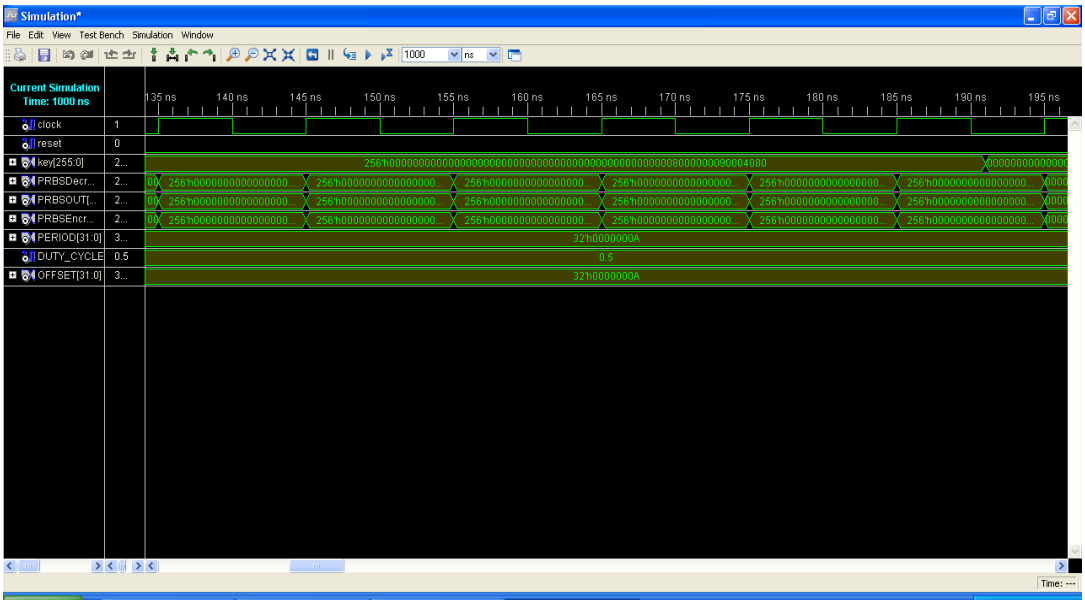
Simulation*
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Current Simulation Time: 1000 ns
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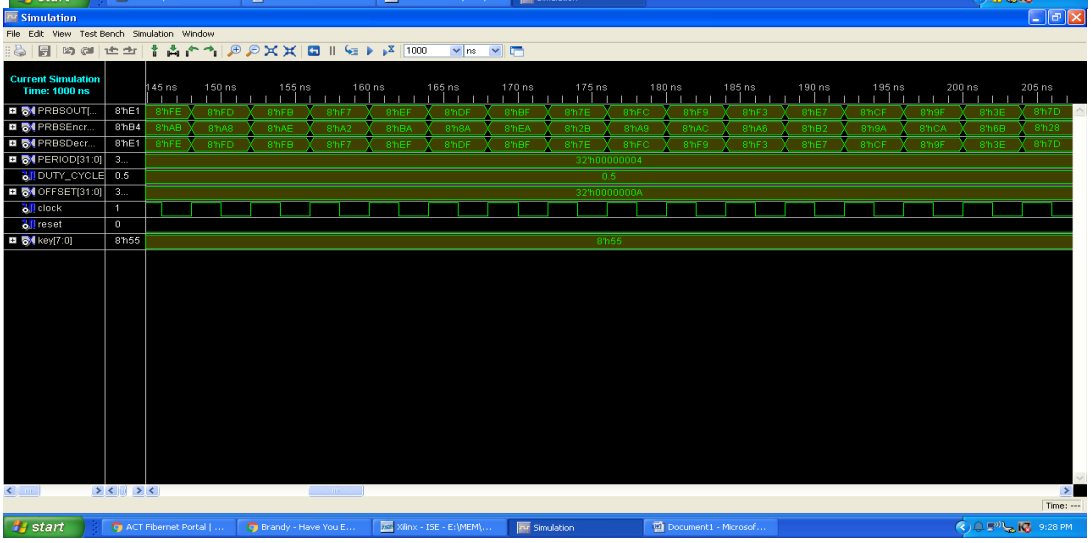
Simulation
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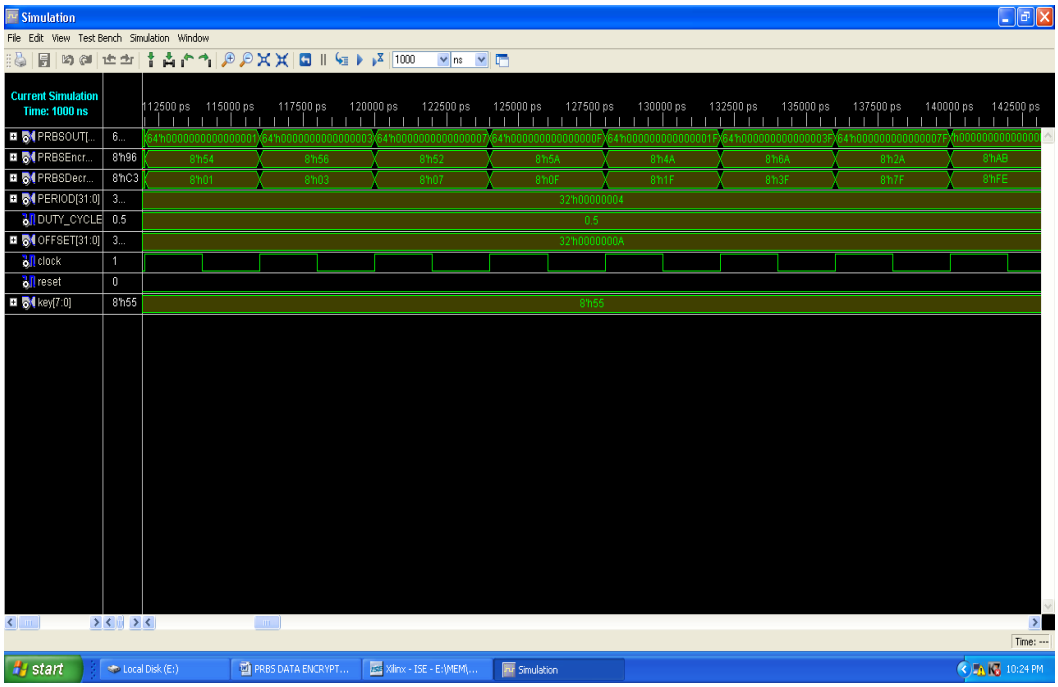
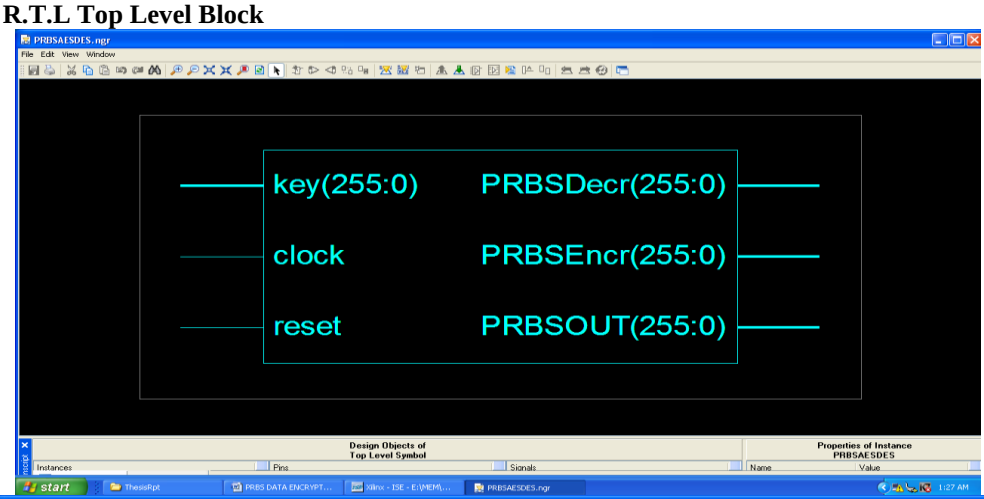
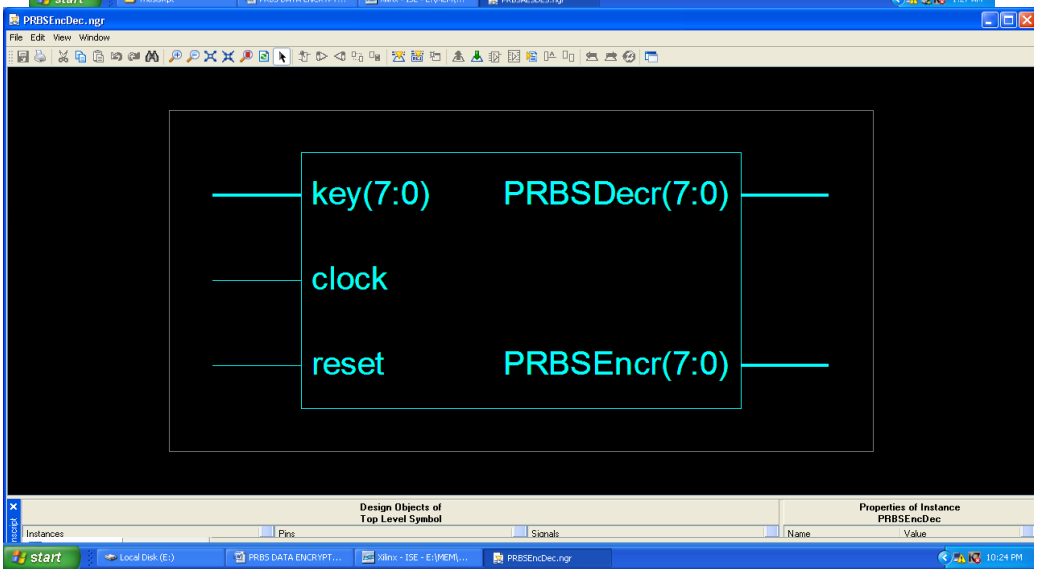


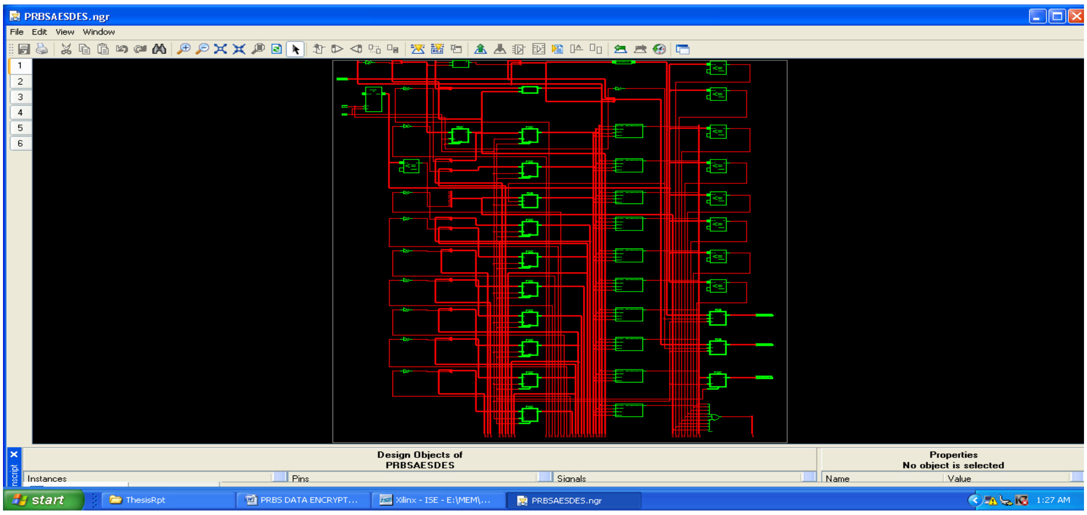
8.1.2 R.T.L. Design Blocks & Schematics - PRBS Data Framer Array Encryption and Decryption

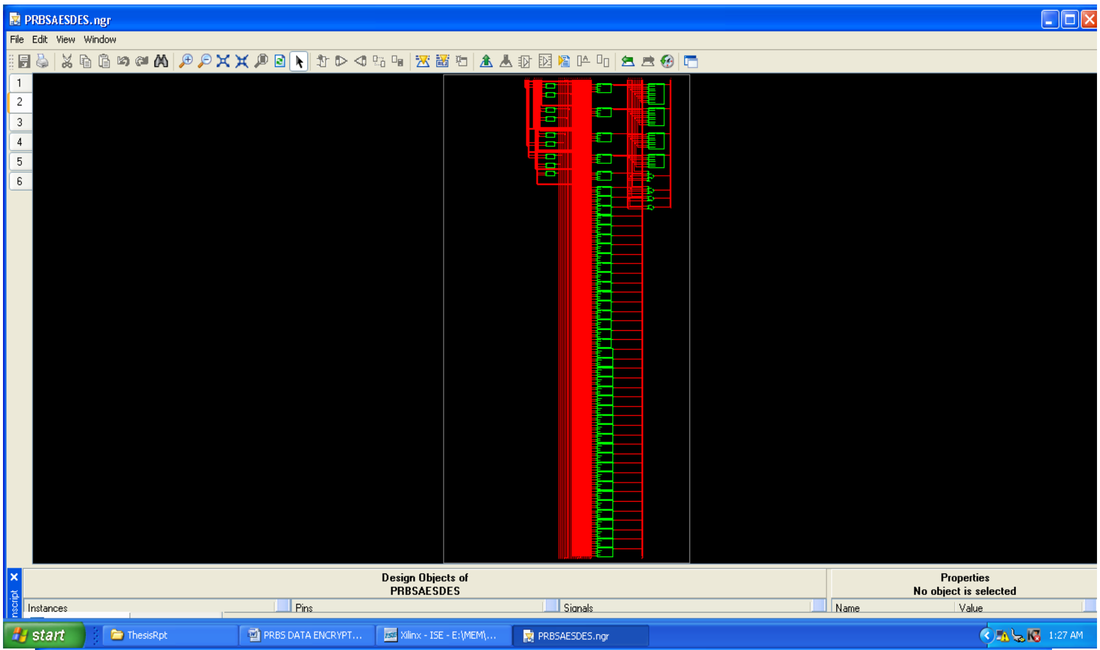
8.1.2.1 R.T.L Top Level Block

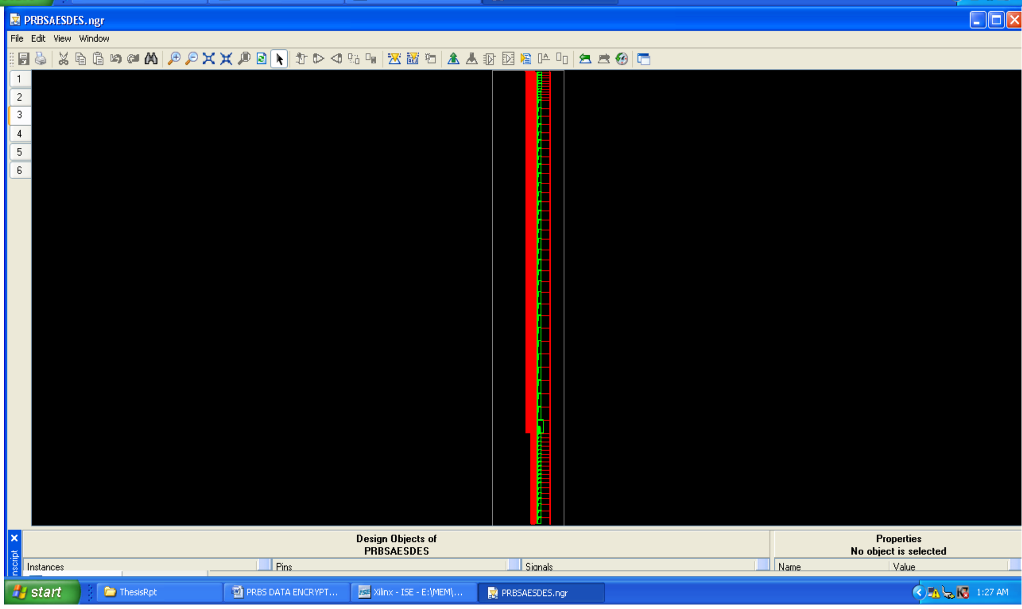


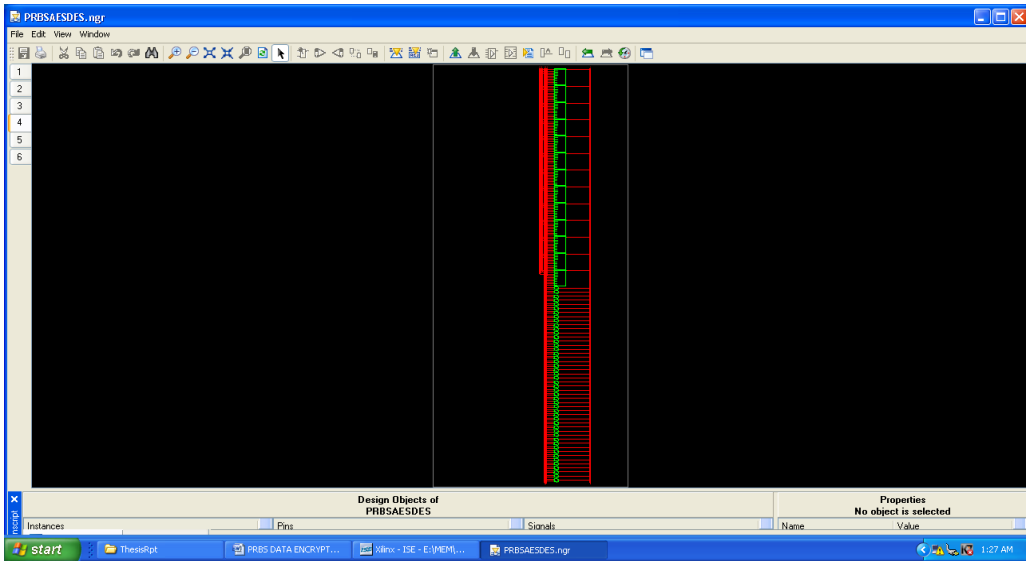


8.1.2.1 R.T.L Schematic





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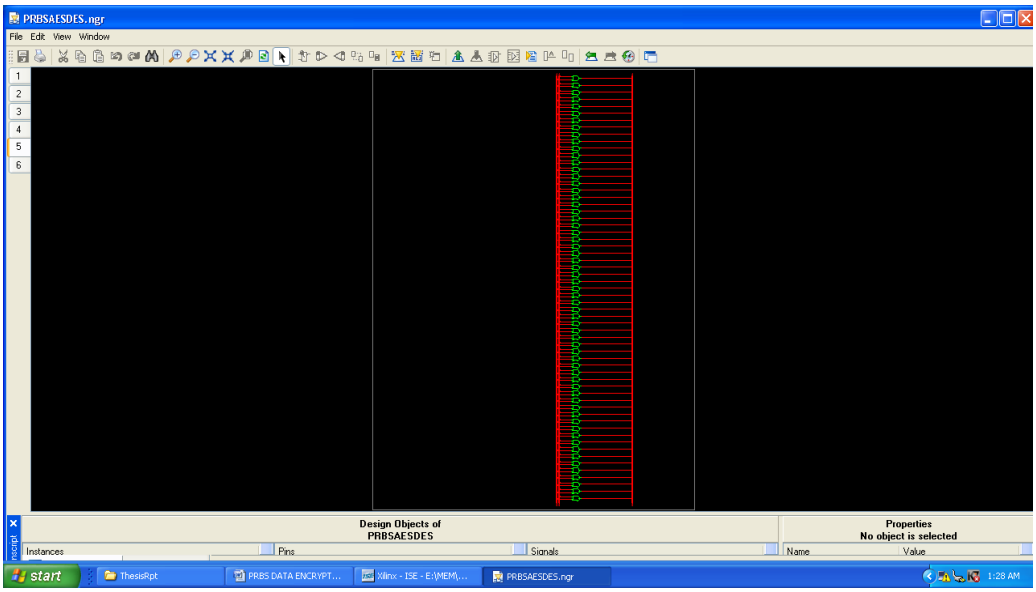
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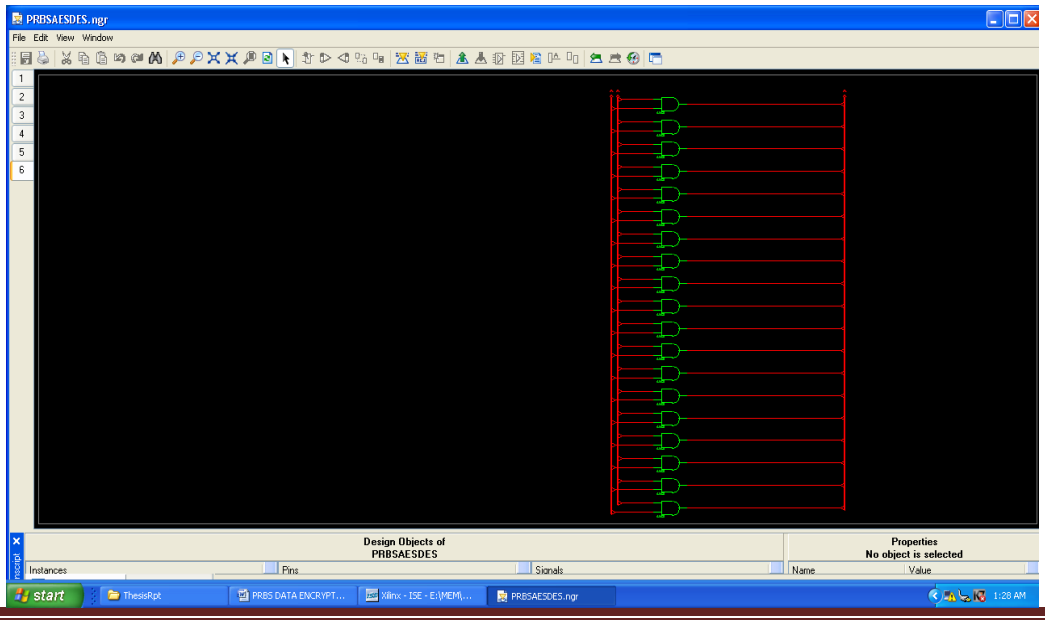
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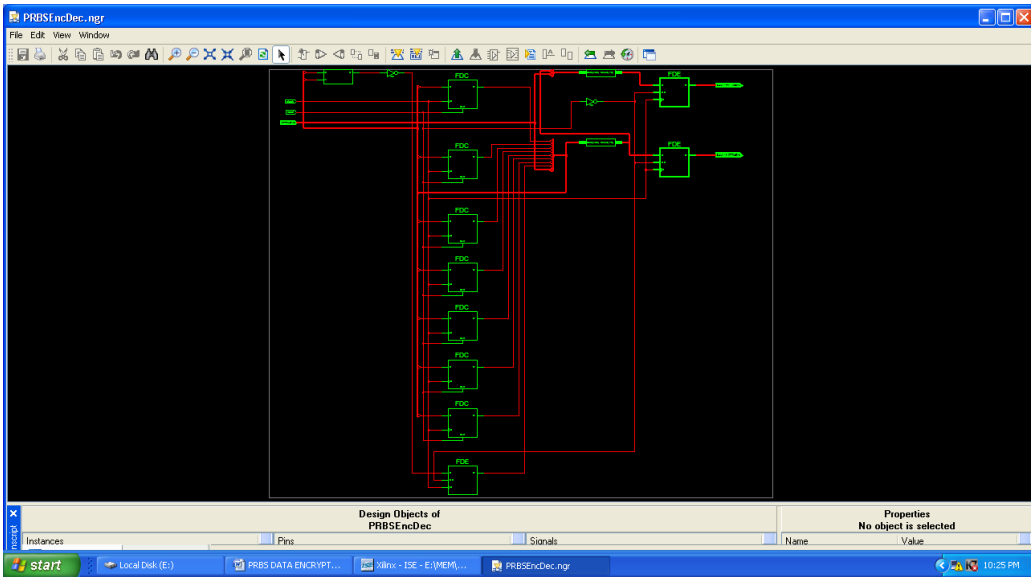
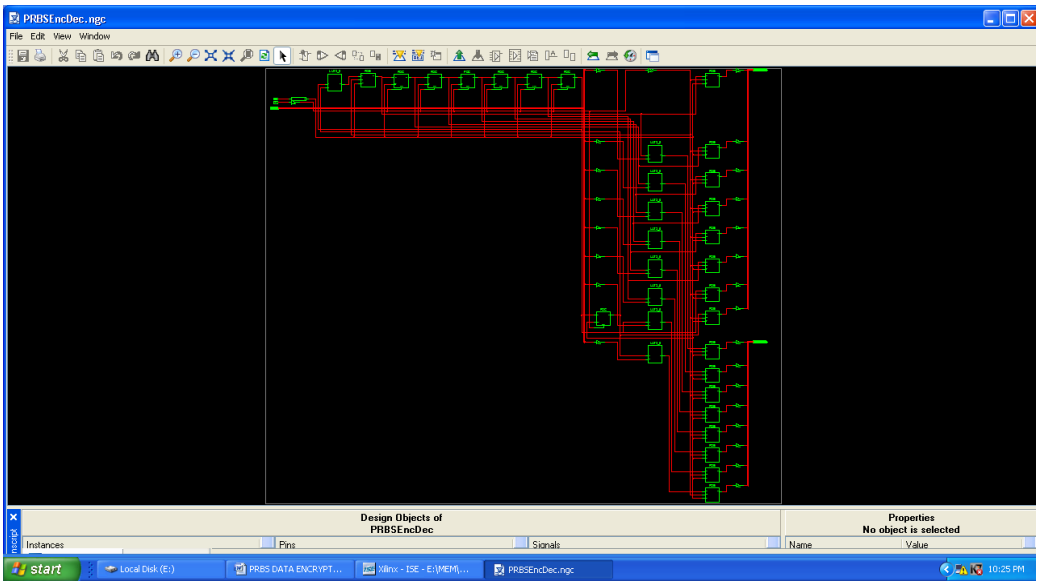
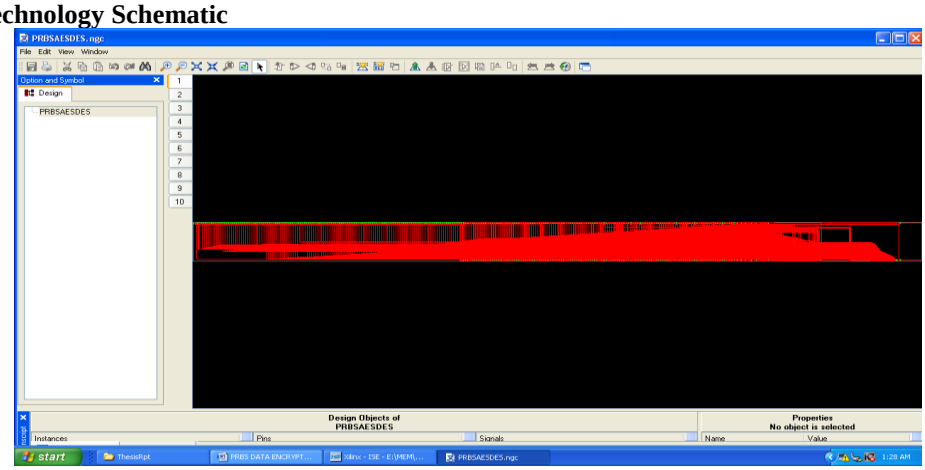
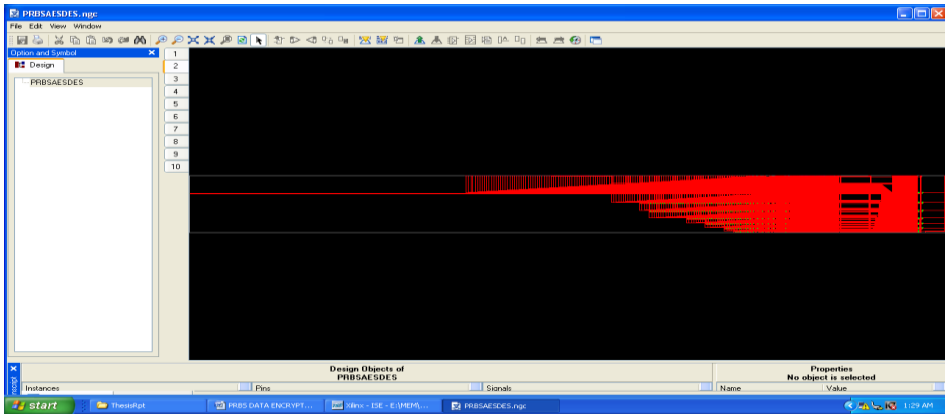




8.1.2.2 Technology Schematic

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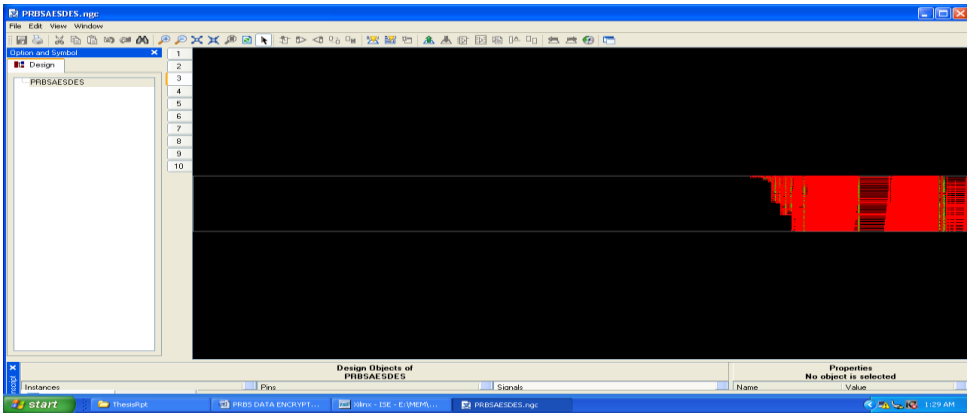
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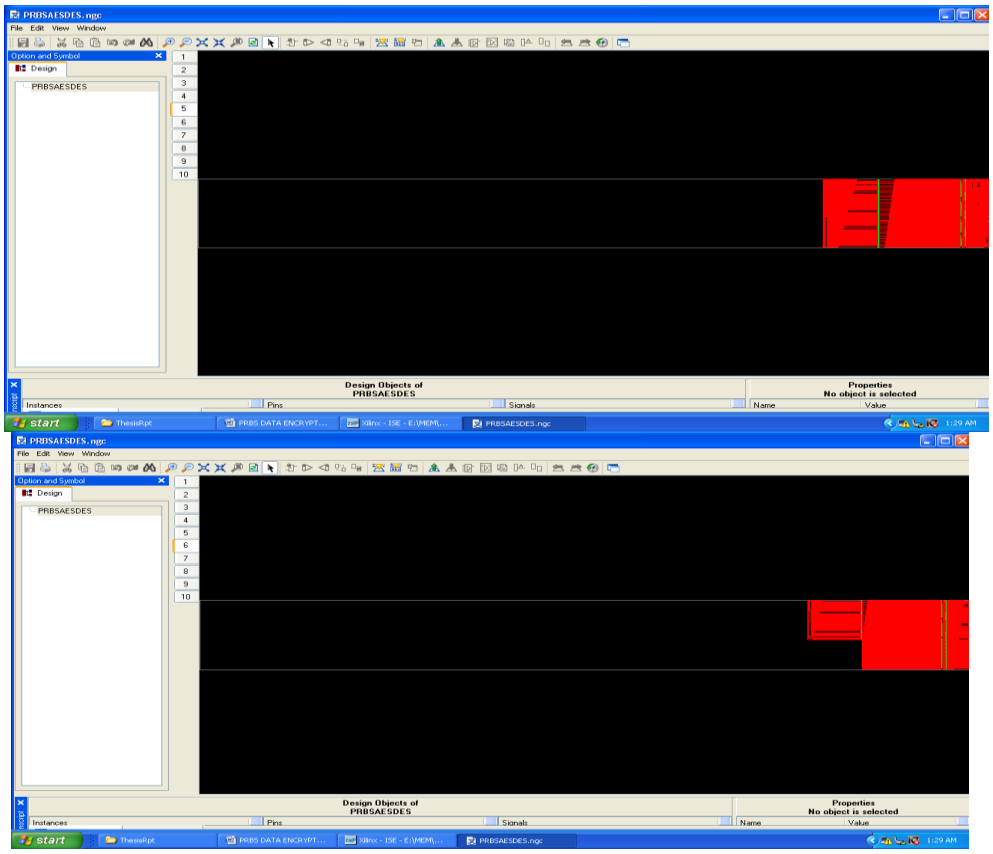
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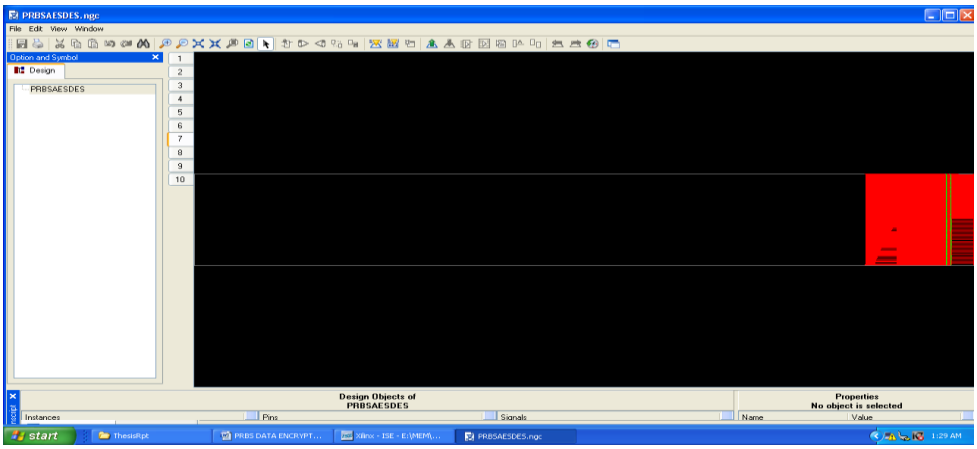
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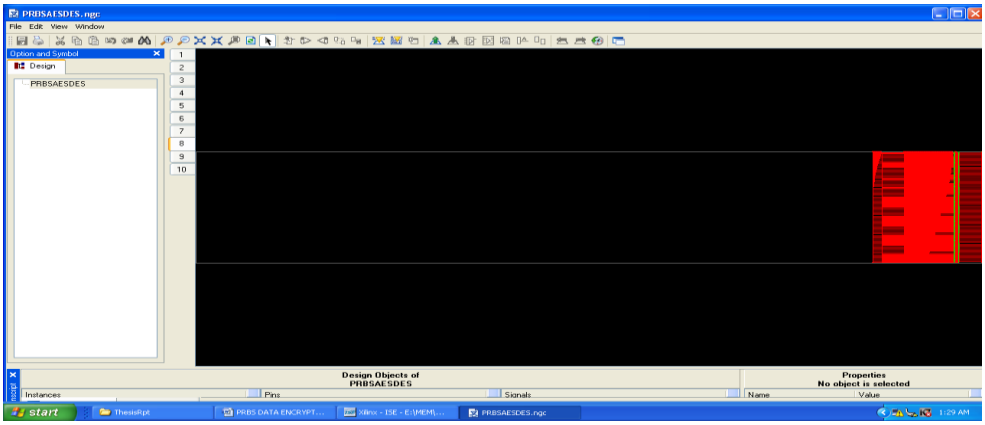
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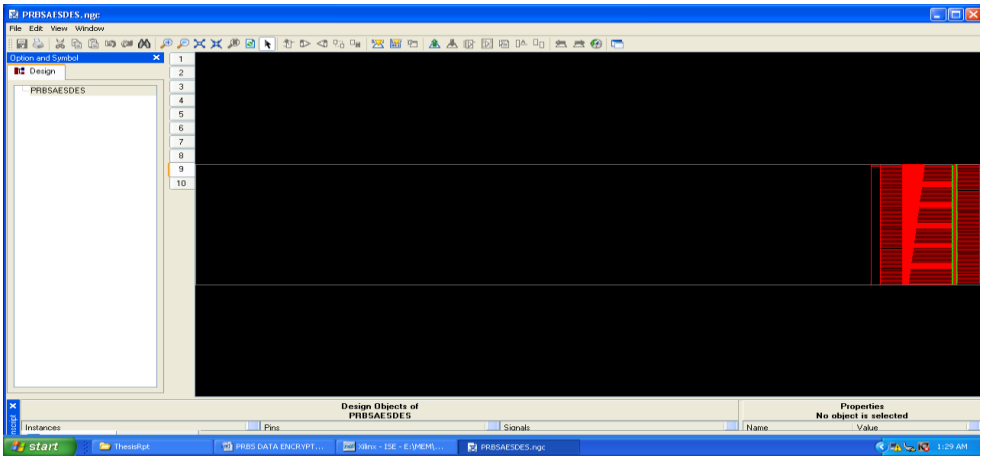
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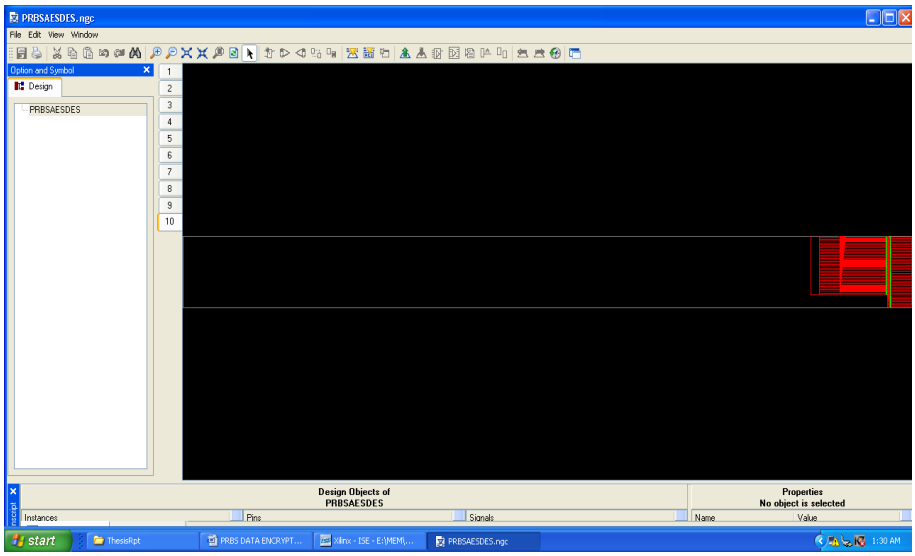
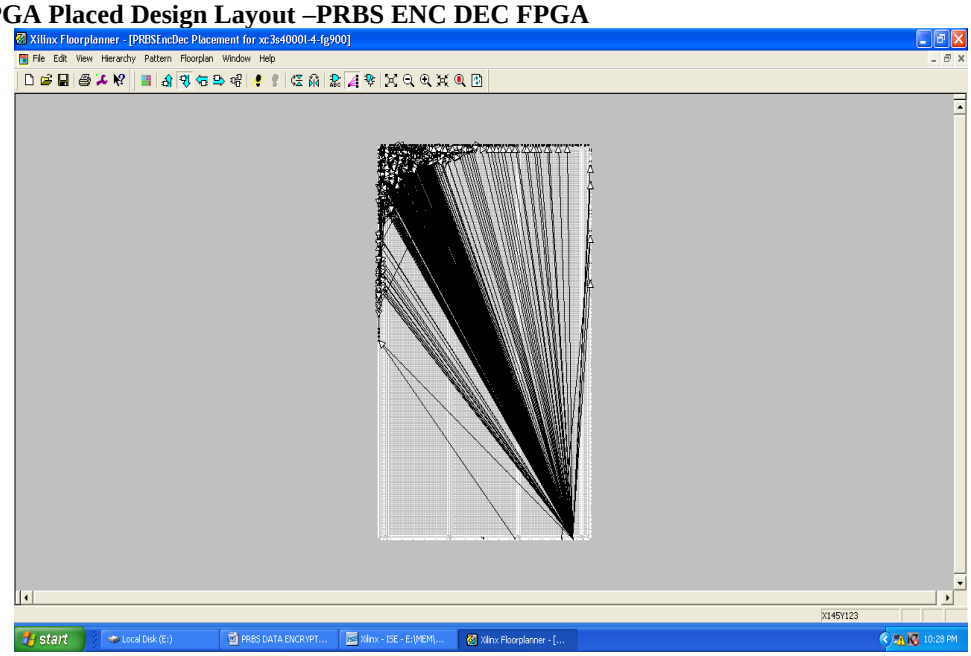
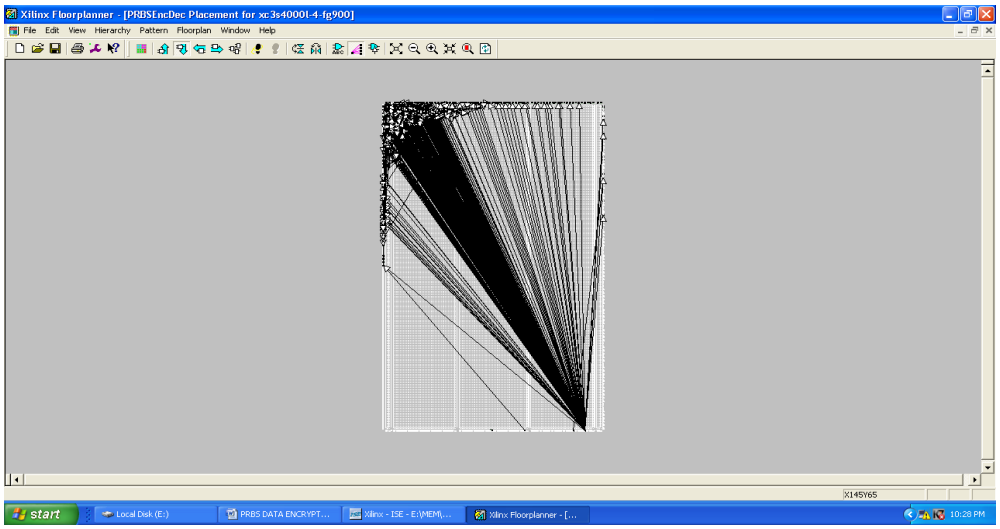
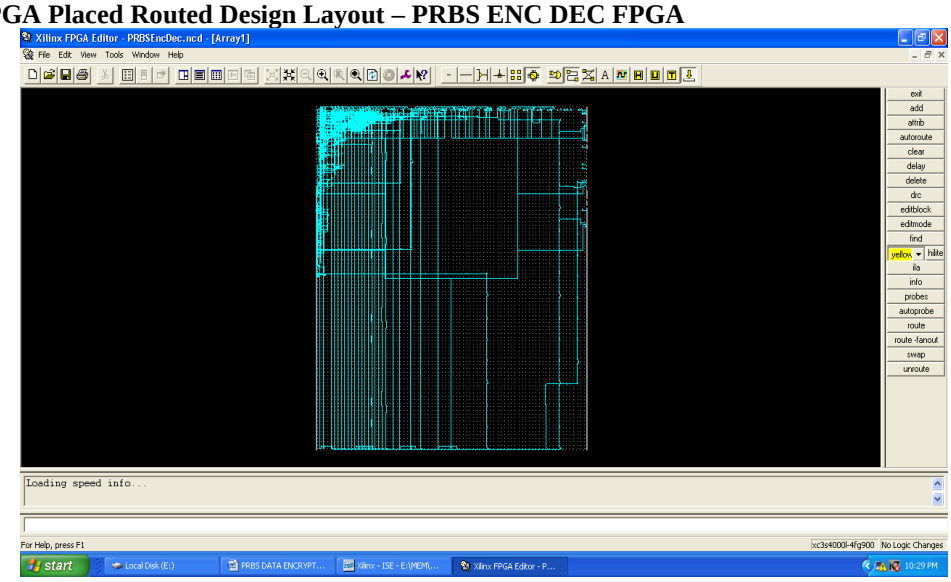


8.1.3 FPGA Placed Design Layout –PRBS ENC DEC FPGA

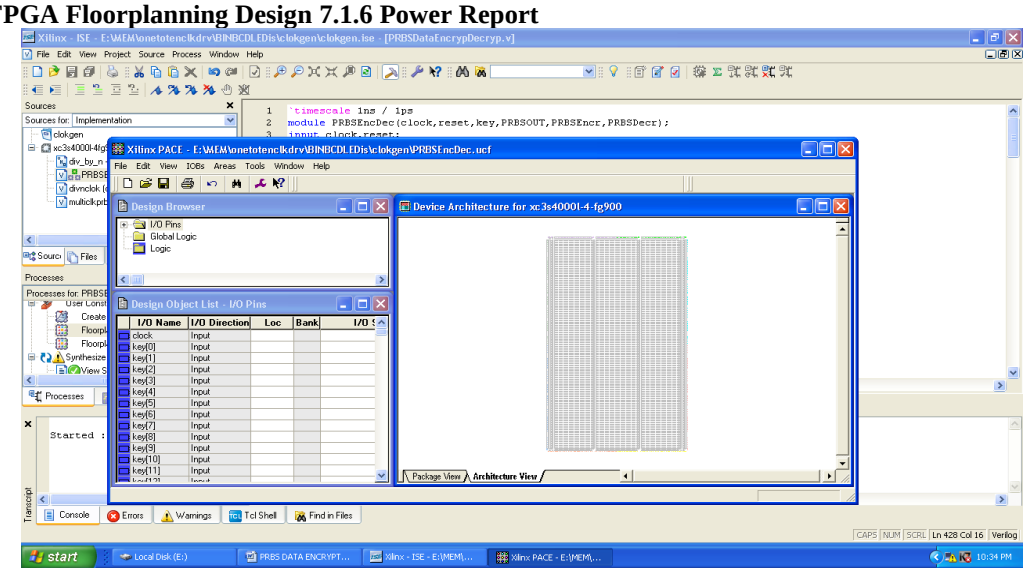


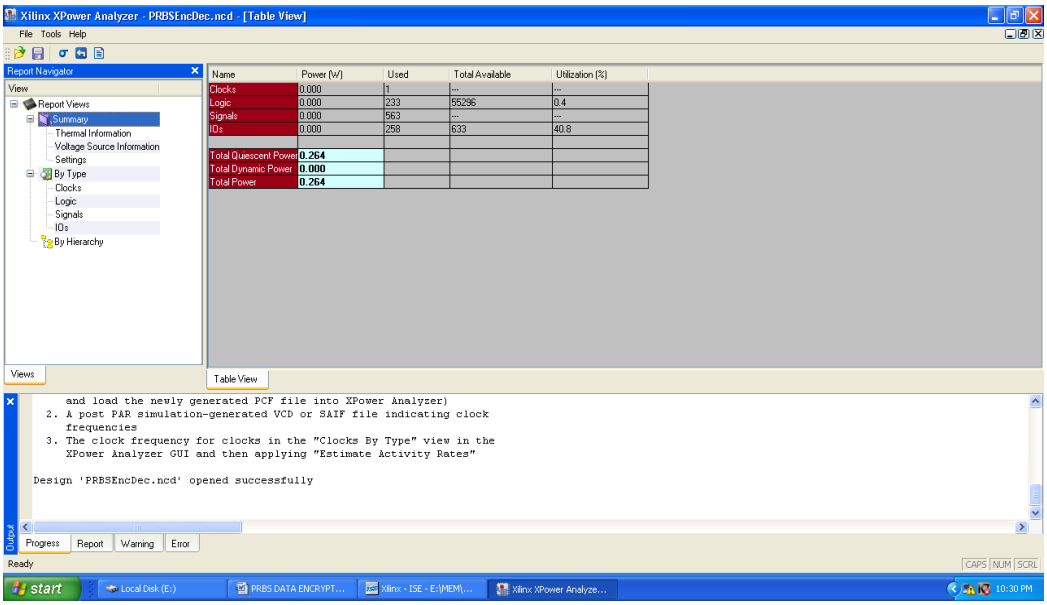


8.1.4 FPGA Placed Routed Design Layout – PRBS ENC DEC FPGA



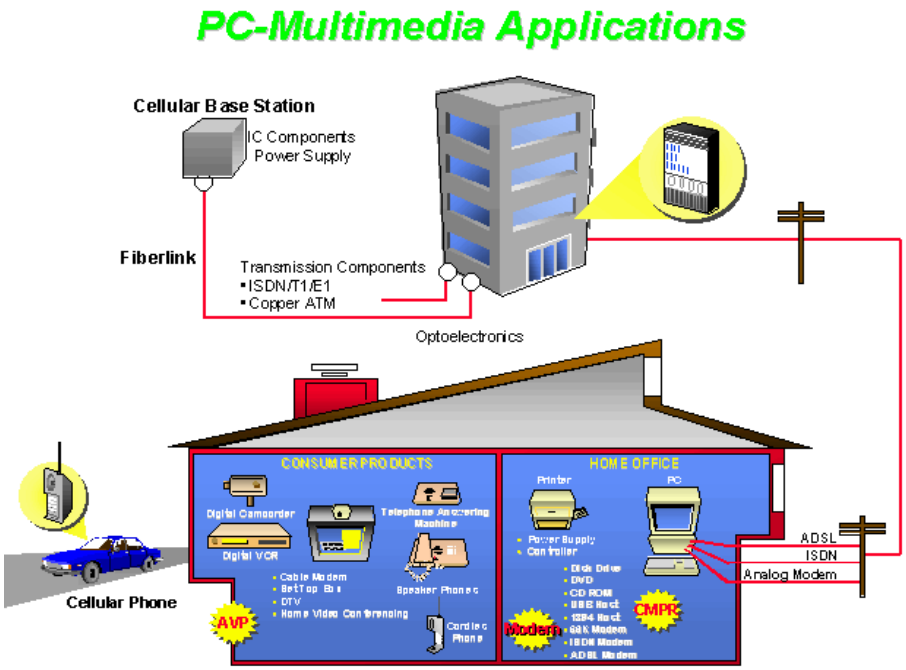
8.1.5 FPGA Floorplanning Design 7.1.6 Power Report

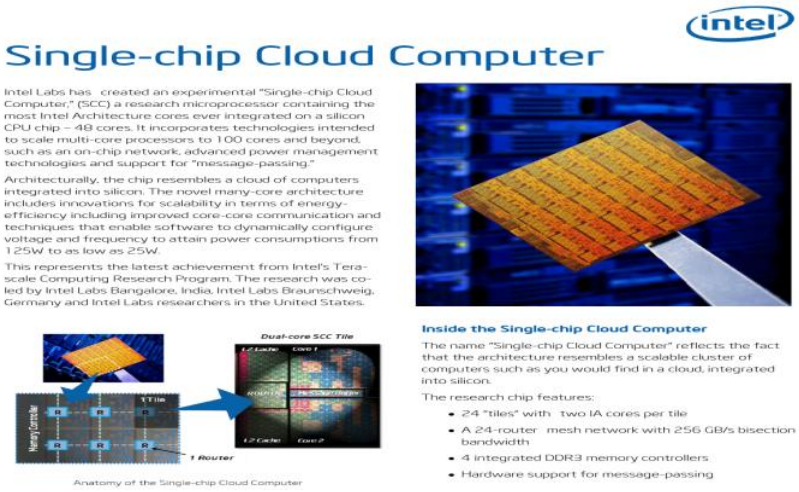


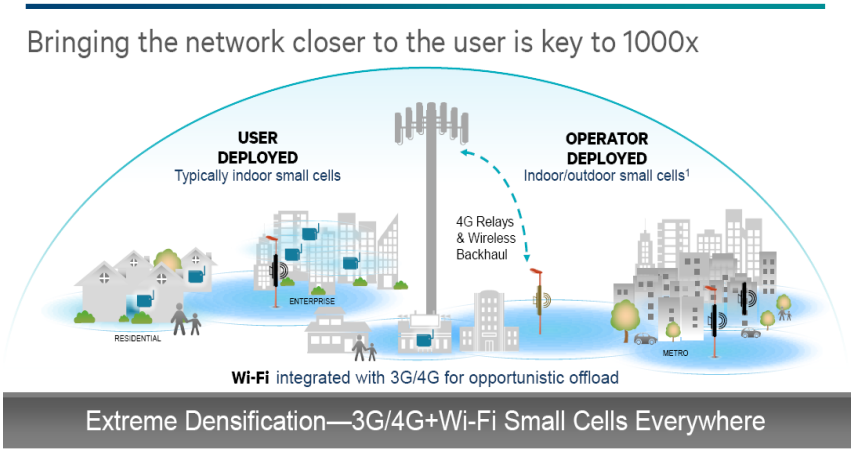


IX. REAL TIME LIVE PRODUCT APPLICATIONS

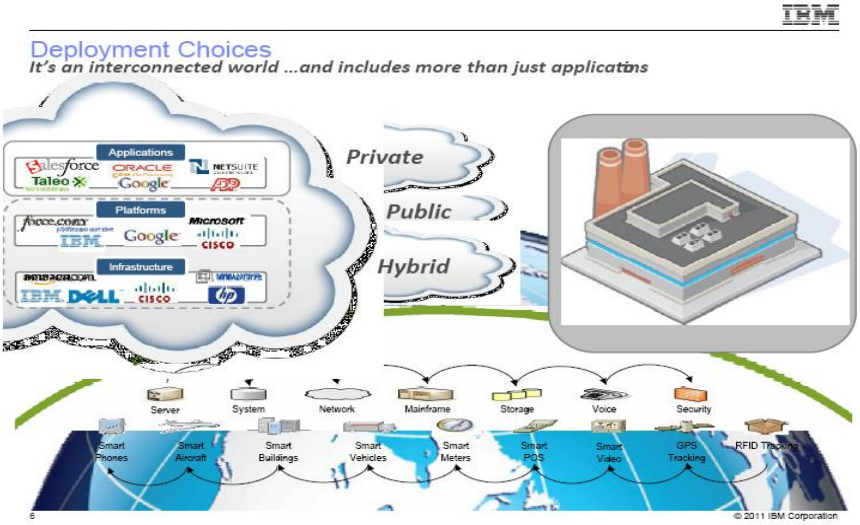
9.1.1 Real Time Live Cloud Computing Applications








iCloud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Smart Meters
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Smart Video
GPS Tracking
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SD
Full HD
4K UHD


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3D Graphics
Video Playback
High Speed Serial Interface
Wireless WAN CDMA &UMTS
TV Out
Security
Music
Imaging & Video
Stereo Headset with Bluetooth/UWB
PC Sync
60 GB HD
Biometrics

X. CONCLUSION

The Design is mainly Intended for increasing the speed of Data Frames and Mainly suit for Big Data base like Cloud, Internet data Computing Applications and Products

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Dr.Vathsal Currently working as a Professor- Aero Dept. I.A.R.E, earlier He Was Dean R&D ,JBIET , He Obtained PhD from I.I.S.C,Bangalore,also Did Post Doctoral Research in DFVLR,Germany and NASA Goddard Space Flight Centre,USA,and also he worked with keen Designations Scientist E,F,G from Reputed Govt R&D Industry Organizations over past years and closely worked with Dr.A.P.J Abdul Kalam He Published lot of various national, international journals & conferences, He guiding 5 PhD Students from Various universities. He Got Prestigious awarded as a Noble Son of India.