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Efficient Approximate Adder Architecture for Error Tolerant Applications with use of new logic values

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----------**ABSTRACT**----------
Ultra-high energy efficiency is required for all the battery operated devices due to increased functionality on the single chip. In conventional digital VLSI design, it is assumed that a circuit/system should function perfectly to provide accurate results.There are many applications which can tolerate small amount of error in their processing e.g. image/video processing, commonly called error tolerant applications.For many digital systems, the data already contained errors. The proposed adder can be efficiently utilized in the image video processing applications. In order to evaluate the efficacy of the proposed adder, proposed and existing adder architecture is implemented on MATLAB to evaluate error metrics and Tanner to evaluate design metrics. Simulation results shows that proposed adder significantly reduces power, area and delay at small loss in accuracy.
Key Word:- VLSI, MATLAB, Image processing, Adder,Highspeed integrated circuits
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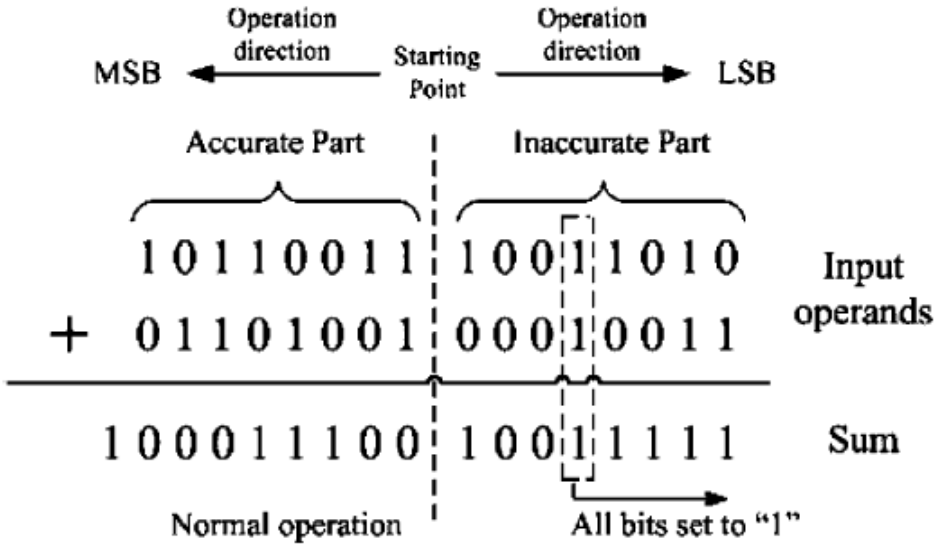
I. INTRODUCTION

Leveraging the applications having error tolerance, we can design adder which provide approximate result very fast compered to conventional design.Small loss in accuracy provides tremendous improvement in power, delay and area. Error Tolerant Adder (ETA) provides high speed by cutting down the carry propagation.ETA can be used in application, which need high speed and may tolerate small error.

Error Tolerant Adder (ETA)

The principle of ETA is to divide adder into: Accurate and Inaccurate partAccurate part includes higher order bits and the inaccurate part includes remaining lower order bits.The addition process starts from the joining point towards the two opposite directions simultaneously

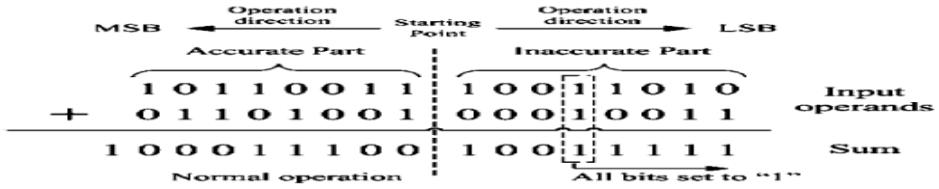


Addition procedure of Error Tolerant Adder

Error Tolerant Adder (cont…)

To minimize the overall error due to the elimination of the carry chain, a special strategy is adapted Check every bit position from left to right, If both input bits are "0"or different, normal one-bit addition is performed and the

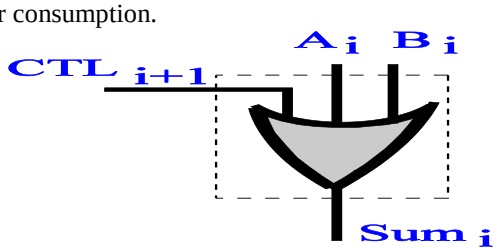
operation proceeds to next bit position, If both input bits are "1", the checking process stopped and from this bit onwards, all sum bits to the right are set to "1".



Addition procedure of Error Tolerant Adder

Proposed Addition Logic

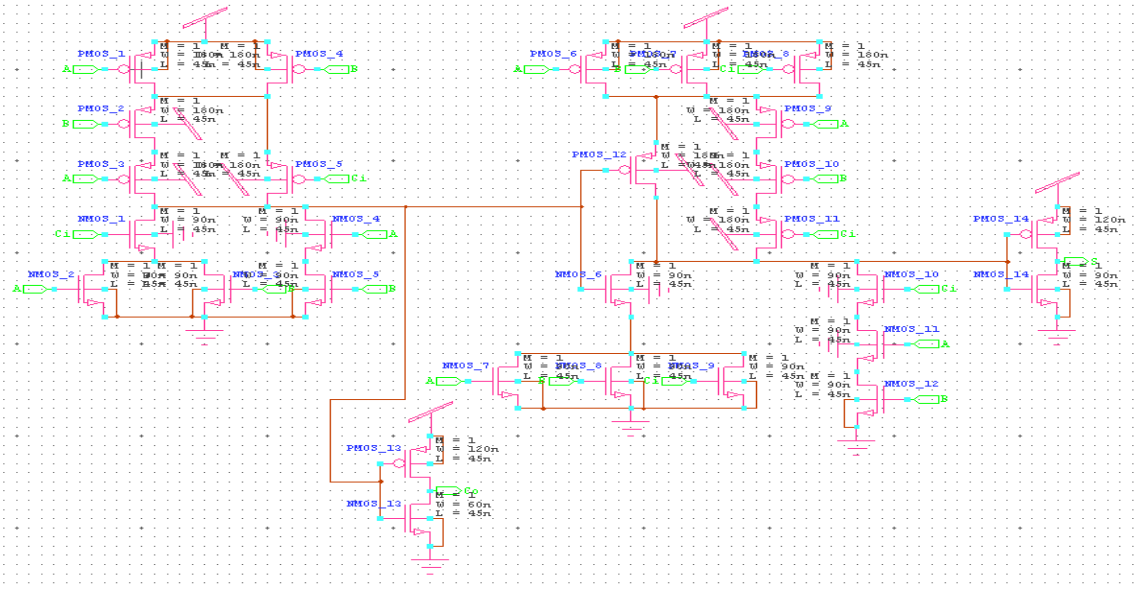
The existing ETA requires large number of transistor to implement approximate sum which in turn increases power consumption. The same functionality can be achieved by the proposed circuit as shown belowThis circuit significantly reduces transistor count (17 in the ETA whereas 8 in the proposed logic i.e. 52.9% reduction) which in turn reduces power consumption.



Proposed m-XOR logic

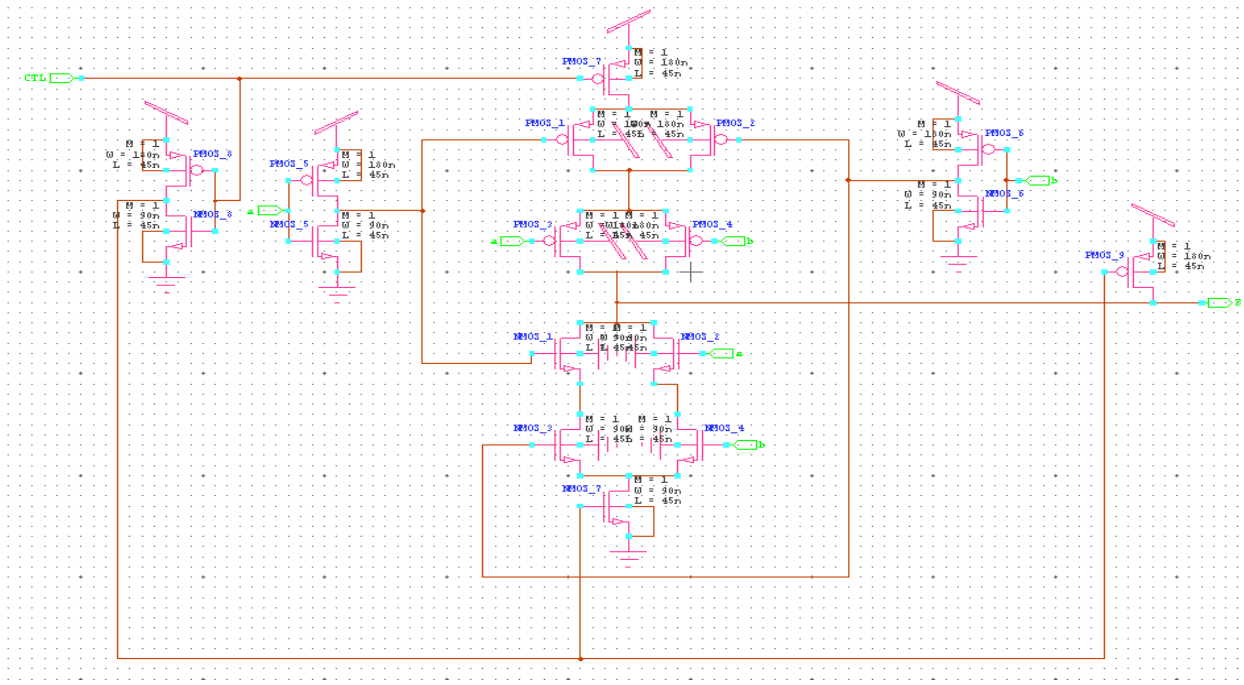
Design Implementation on Tanner

Schematic of Full Adder on Tanner



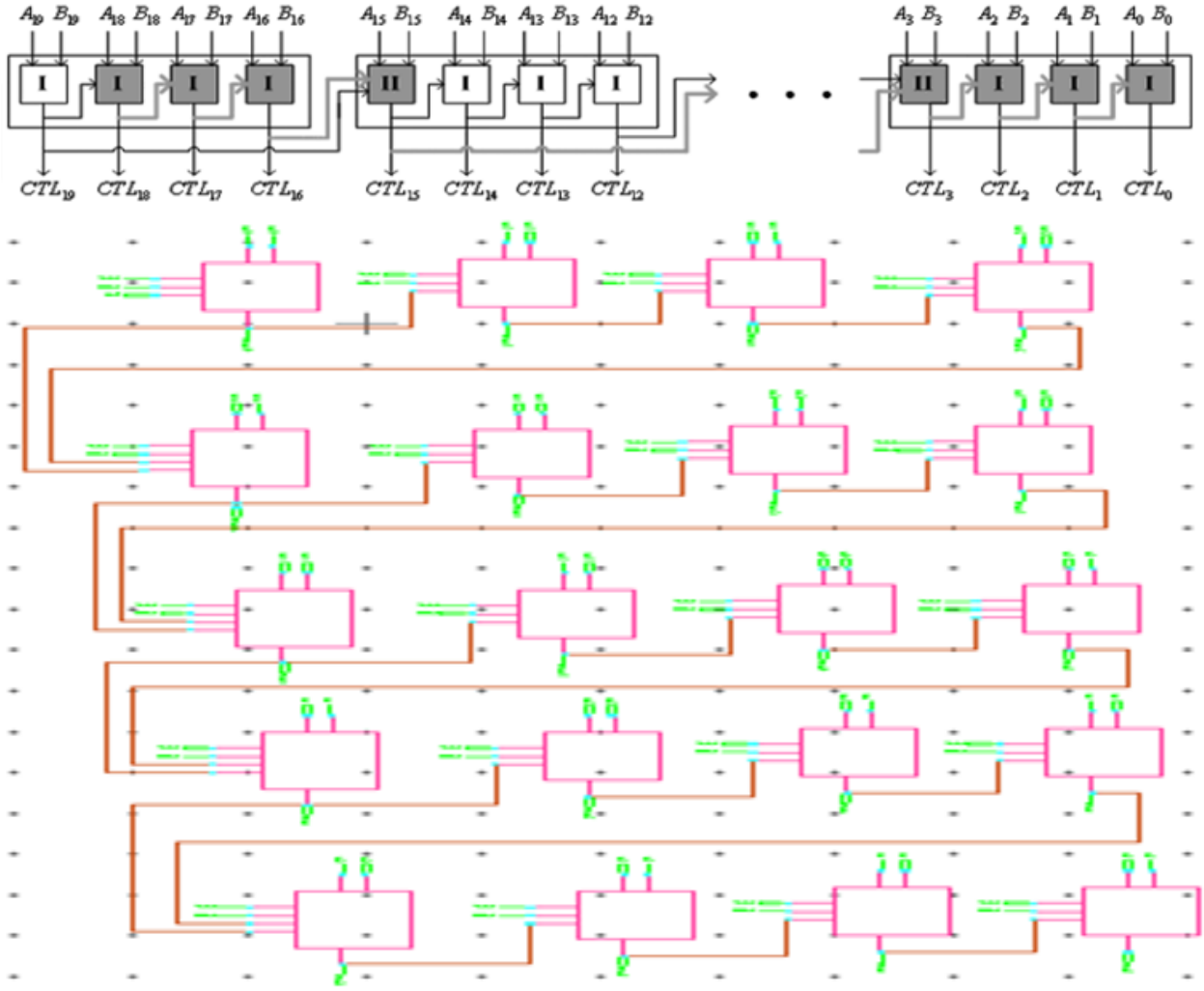
Schematic 28T diagram of Full Adder

ETA implementation: Modified XOR



Schematic of Modified XOR implemented on Tanner

ETA implementation: Control block



Result

Design Metrics Comparison: 8-bit Adders

Type of Adder	Power (uw)	Delay (ns)	PDP (fJ)	Transistor Count
ETA	1.85	0.134	0.247	222

Design Metrics Comparison: 16-bit Adders

Type of Adder	Power (uw)	Delay (ns)	PDP (fJ)	Transistor Count
ETA	2.56	0.305	0.78	542

Design Metrics Comparison: 32-bit

Type of Adder	Power (uw)	Delay (ns)	PDP (fJ)	Transistor Count
ETA	5.18	0.616	3.19	912

Conclusion

Approximate adder in these application significantly improves the design metrics at the cost slightly degradation in quality.Simulation results on the Tanner shows that ETA exhibits significant improvement over the accurate adder architectures.MATLAB simulation results shows very small amount of error.Thus ETA can be effectively applied in the image/video processing applications

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