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Design of a Low Noise Amplifier using 0.18µm CMOS technology

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ABSTRACT

This paper presents an unconditionally stable Low Noise Amplifier for the L1 carrier of Global positioning system signal (GPS) operating on the 1.57542 Ghz band. A supply voltage of just 1 V is used here. Work is done on the Cadence Virtuoso platform and the performance parameters like Noise Figure, Gain, Reverse Isolation, extent of input as well as output matching, linearity are all simulated and plotted. It is observed that a tradeoff between the various parameters is necessary.

INDEX TERMS—*Gain, Inductively degenerated LNA, Low Noise amplifier, Noise figure.*

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I. INTRODUCTION

GPS signals are very weak signals. A typical GPS signal received at the earth station have a power of around -135 dBm. This is an extremely small value. Therefore, the design of a Low Noise Amplifier in accordance with the specified values of Noise figure and Gain is crucial. From Friis transmission formula it is observed that the noise figure of the entire receiver is mostly influenced by the first stage itself if the Gain is sufficiently high. This parameter, coupled with a low noise figure is the main aim of a good low noise amplifier design.

In this paper, a low voltage CMOS LNA is designed for the GPS L1 band. Work is done one the Cadence virtuoso platform using the tsmc18 library. They layout is also design with zero errors in both the Design Rule Check (DRC) and Layout vs Schematic check (LVS) implying that the design is ready for fabrication.

II. LNA DESIGN

The final and complete schematic of the LNA is shown in Figure 1. Here all the inductors

(L1,L2,L3) are implemented as on chip spiral inductors. Amongst all the input matching methods namely resistive termination, series shunt feedback, common gate and inductive degeneration, the last one is selected simply because it offers the lowest noise figure. The minimum noise figure in resistive termination is 3 dB because of the thermal noise offered by the resistor at the gate of the transistor. The minimum noise figure offered by common gate configuration is 2.2 dB even though no resistors are present here. Inductive degeneration topology offers the lowest noise figure and no resistors are required here. It is called inductive degeneration because the L3 inductor is connected in such a way that the current through it opposes the current through the gate of the transistor M1 (negative feedback). This negative feedback connection is vital because it provides the necessary stability the circuit needs as well as improves a wide array of parameters.

The transistor M2 is connected in common gate connection and the transistor M1 is connected in common source connection. Together they form a cascode, this cascode connection is necessary to provide the required isolation between the input and the output, reduce the effect of miller effect caused by gate-drain capacitance Cgd of the M1 transistor. The inductors L1 and L3 are chosen in such a way as to provide matching to the output resistance of the antenna (50Ω in this case). Their combination forms the input resistance (Rs) where is matched to the output of the antenna for favorable results.

The transistor M3, R1 and R2 forms the biasing circuit. They are used to set the prerequisite DC voltage so that the transistor can operate in the correct region (Region 2 in this case). Transistor M1 forms a current mirror with the transistor M3, whose width is just a fraction of the width of M1 to minimize the current through it and hence save power. The current through the transistor M3 is set by the supply voltage as well the resistor R1 which is chosen to be around 500Ω. The resistor R2 has to be large enough so that the equivalent noise current is small enough to be ignored. Here it is chosen to be around 5KΩ (optimized). The capacitor C3 forms the final piece of the DC biasing circuit. It acts a DC blocking capacitor and should be large enough to provide a negligible reactance at the frequency if 1.57542 Ghz. Here it is chosen as 1.2pF.

The inductor L2, Capacitor C2 and the resistor R3 form the output matching circuit. Output matching is once again crucial so as to provide maximum power to the subsequent stage of the LNA which is usually a mixer or in some cases a band pass filter for image rejection. Together they form a parallel tank circuit as opposed to a series tank circuit at the input of the transistor M1.

Supply voltage used here is just 1V. At the input of the LNA an AC source with a sweep of -10dbm and an amplitude of 1V is modeled. The resistor R3 is known as the output loading resistor which provides stability but reduces the gain as well as the compression point.

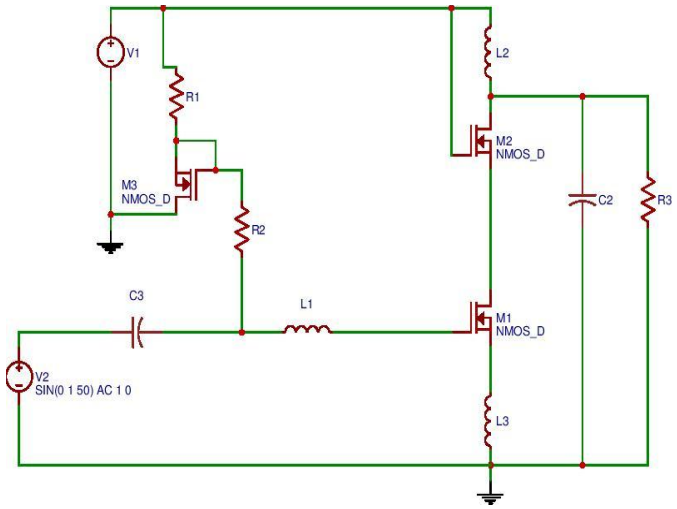

Figure 1: LNA Schematic

III. COMPONENT DESIGN

STEP 1: ***Calculation of gate-oxide Capacitance (Cox)***

$$C_{ox} = \frac{\varepsilon ox}{tox}$$

$$\varepsilon_{ox} = \varepsilon_0 \text{ x } \varepsilon_r$$

Here, ε_{ox} = Permittivity of gate oxide,
t_{ox} = Thickness of gate-oxide,
ε_0 = Free space permittivity,
ε_r = Relative permittivity.

We know , $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m,
$\varepsilon_r = 3.9$

Hence we get,
$\varepsilon_{ox} = 3.45 \text{ x } 10^{-11}$ F/m

so,

$$C_{ox} = \frac{3.45\ X\ 10\text{^}(-11)}{4.1\ X\ 10\text{^}(-9)} = 8.42 \text{ x } 10^{-3} \text{F/m}^2.$$

STEP2: ***Calculation of optimum width of the transistor M1***

$$W_{opt} = \frac{1}{3.Cox.\omega.L.Rs}$$

Where C_{ox} = Capacitance of the gate-oxide,
ω = Angular frequency,
L = length of the device,
R_s = Source resistance.

Hence we obtain,

$$W_{opt=} \frac{1}{3(8.42\ X\ 10^{-3})X(\ 2\Pi\ X\ 1.57542\ X\ 10^{9})X(\ 180\ X\ 10^{-9})\ X\ (50)}$$

$$\approx 444\mu\text{m}.$$

STEP 3: ***Calculation of gate-source capacitance (Cgs)***

$$C_{gs} = \frac{2\ X\ Wopt\ X\ Cox\ X\ L}{3}$$

Substituting the values W_{opt} = 444µm, C_{ox} = 8.42 x 10^{-3}F/m and L = 180nm, we get

$$C_{gs} \approx 449 \text{ fF}.$$

STEP 5: ***Calculation of Source inductor L3***

We know the input impedance looking into the LNA as:

$$Z = j\omega Ls + \frac{gm.Ls}{Cgs} + \frac{1}{j\omega Cgs};$$

The individual inductance and capacitance part would be resonated out and the remaining part should be effectively equal to 50Ω, so we get,

$$\frac{gm.Ls}{Cgs} = 50$$

Substituting the values of g_m and C_{gs} in the above gives us L_s = 400 pH.

STEP 6***: Calculation of Gate inductor L1***

We are employing a series resonant circuit at the input, to set the resonant frequency. The resonant frequency of a series resonant circuit is as follows:

$$f = \frac{1}{2\Pi\sqrt{(Ls+Lg).Cgs}}$$

Substituting the obtained values of L_s and $C_{gs,}$ we get a value of $L_g \approx 22$ nH.

STEP 7: ***Calculation of output inductor***

The equation that governs the output matching is as follows:

$$Z = g_m r_{ds} Z_s + Z_s + r_{ds}$$

Where g_m is the transconductance,

r_{ds} is the drain to source resistance,

Z_s is the source impedance.

The formula for the resonant frequency of a parallel resonant circuit is as follows:

$$F = \frac{1}{2\Pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}$$

We need to work on the formula of Z twice as we have two cascaded amplifiers, by substituting the values of g_m r_{ds}, Z_s, R and C values of the parallel resonant circuit we obtain the value of L as approximately 17.7 nH.

IV. RESULTS

Using standard CMOS 180nm tsmc18 library, the LNA is designed and implemented for 1.57542Ghz. Simulation is done on the Cadence virtuoso platform.

1. Noise Figure

The width of the transistor M3 is just a fraction of the width of the transistor M1. Since the width of the transistor M1 was derived to be 444µm the width of M3 is just 2.1µm. To implement the transistor with 444µm as its width, 60 fingers are used, with the width of each finger being 7.4µm. The current mirror can be discarded at the cost of extra power supply for biasing. For these parameters a noise figure of just 1.15dB is obtained. In figure 2 a graph between noise factor in db(noise figure) and frequency is plotted.

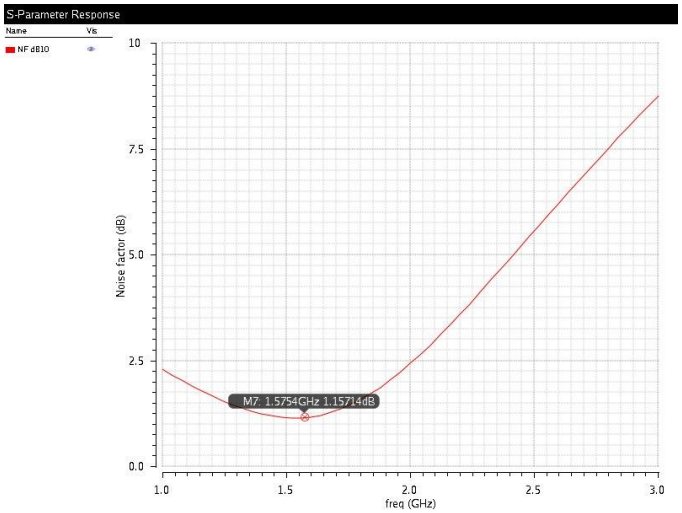

Figure 2: Noise figure vs frequency

2. S parameters

The isolation obtained from the proposed LNA is one of the best in the business. The figure of merit for this is the Reverse transmission gain given by S12. A value of -36.74dB is obtained. The gain so obtained is sufficiently high for the LNA design to be feasible. The gain (S21) when measured at port 2 is found to be 18.9dB.

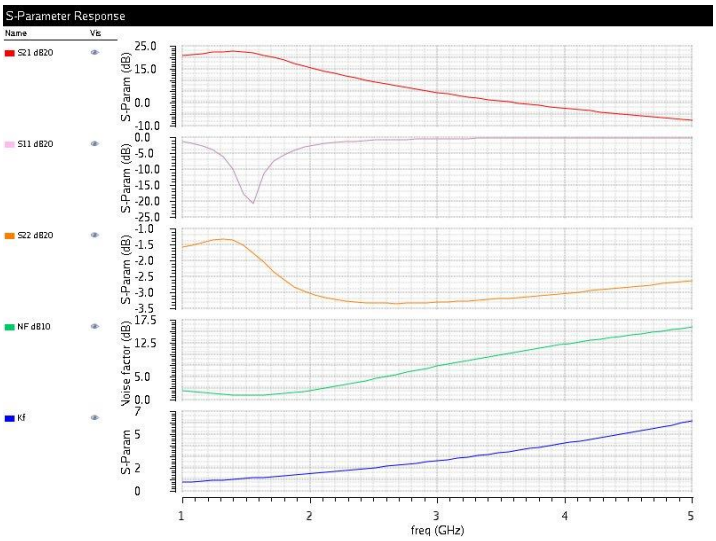

Figure 3: S parameters

3. Stability Factor

The stability of the circuit is determined by the Rollet's stability factor. If the value so obtained is greater than 1 then the circuit is said to be unconditionally stable. For this design a value of 1.53 is obtained implying stability no matter what the load is.

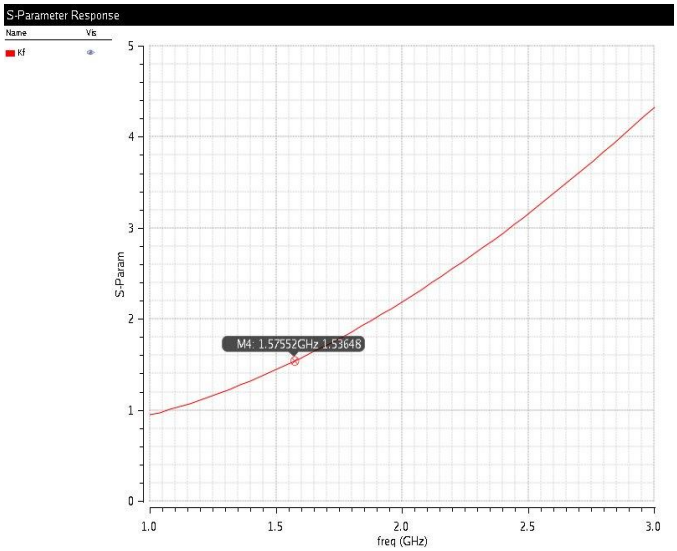

Figure 4: Stability Factor

4. Linearity

Linearity is a measure of how well output follows the input. 1 dB compression point and IIP3 figures of merit for linearity of an LNA. The third order intercept point gives an idea of how well a receiver performs in the vicinity of strong signals. Since the signal received from the satellites is of the order of -135dBm the IIP3 must be as high as possible. For this design the IIP3 occurs at -28dBm which is a reasonable value.

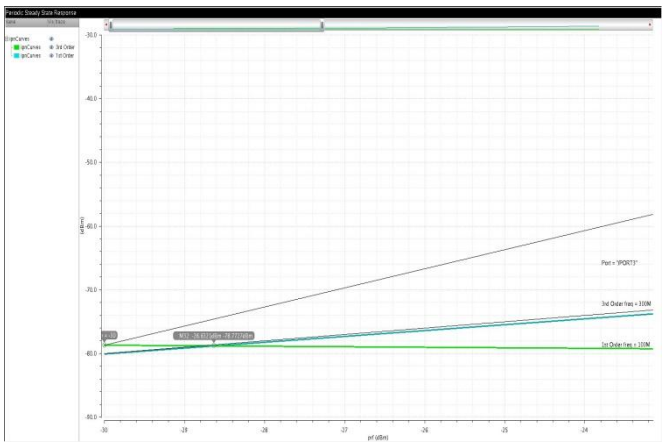

Figure 5 : Linearity

The results given above are summarized in the table below:

S. No.	Property	Results
1.	Technology	CMOS 0.18µm
2.	Noise figure	1.15715dB
3.	Gain	18.9159dB
4.	S11	-13.1522dB
5.	S12	-36.7451dB
6.	Rf Frequency	1.57542Ghz
7.	Supply	1V
8.	Power	11mW
9.	K factor	1.53648

Table 1: Specifications

V. CONCLUSION

A low voltage CMOS LNA was designed using CMOS 180nm technology on the tsmc18 library of the Cadence virtuoso platform. The designed LNA exhibits a gain of 18.91 dB; S11 of -13.1522dB and exhibits unconditional stability. The layout was also designed with zero errors in both DRC (Design Rule check) and LVS (layout vs schematic check) implying that the proposed LNA can be fabricated without any off-chip components.

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