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A concept paper on "On Chip High Voltage generator using Polysilicon Diodes"

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----------ABSTRACT----------
In this Paper an On chip High Voltage Generator with bulk CMOS process using Polysilicon Diodes is presented. As the polysilicon diodes are completely isolated from the bulk so the output voltage is not limited by the junction breakdown voltage of CMOS in charge pump circuit. The output voltage of voltage generator realized by this technique is much higher than n well/p well substrate breakdown voltage with standard CMOS process.

KEYWORDS: *Breakdown ,Charge pump, CMOS , Polysilicon, Isolated trench, SOI*

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I. INTRODUCTION

Charge pump circuit generates the dc voltages which are higher than the normal power supply voltage (VDD) or lower than the ground voltage (GND). Charge pump circuit are generally applied to the nonvolatile memories. Beside this , charge pump circuits can also be used in some low-voltage design to improve the circuit performance . In the MEMS applications, the charge pump circuit have to provide the output voltage higher than 15 V , early, the pn-junction diodes were used . Then, Dickson introduced the charge pump circuit by using the diode connected devices . But due to the body effect, the pumping efficiency of the Dickson charge pump circuit degrades as the number of the stages increases.[5-6] Several modified charge pump circuits based on the Dickson charge pump circuit are reported for enhancing the pumping efficiency .[1]

As the semiconductor process is scaled down, the normal operation voltage of MOS also decreases due to the reliability issue. So, the reliability issue should be considered to design the charge pump circuit in the deep-sub-micron process. Figure 1(a) shows the cross section of the p+/n-well diode with the grounded p-substrate. In Figure 1(a), a parasitic pn-junction is present between the n-well and the p-type substrate. Here , if the voltage on the cathode of p+/n –well diode is greater than the junction breakdown voltage between n-well and substrate than leakage current will arise. Figure 1(b) shows the diode connected NMOS, whose gate and drain are connected together, in the grounded p-substrate. In this Figure , an undesired pn-junction is present between the n+ region (source/drain) and the grounded p-substrate. Here also , if the voltages on the cathode or anode of the diode-connected NMOS are larger than the junction breakdown voltage between the n+ region (source/drain) and the grounded p-substrate, the charge leakage will occur. Thus, whenever the p+/n-well (pn-junction) diodes or the diode-connected devices are used , the output voltage is limited by the breakdown voltage of the undesired junction in standard CMOS process. [2-4]But with the use of SOI (silicon-on-insulator) process, the charge pump circuits can pump the output voltage higher without the limitation because the devices in the SOI CMOS process are isolated from others by the insulator layer . However, the SOI CMOS process is much expensive than the standard CMOS process.[1]

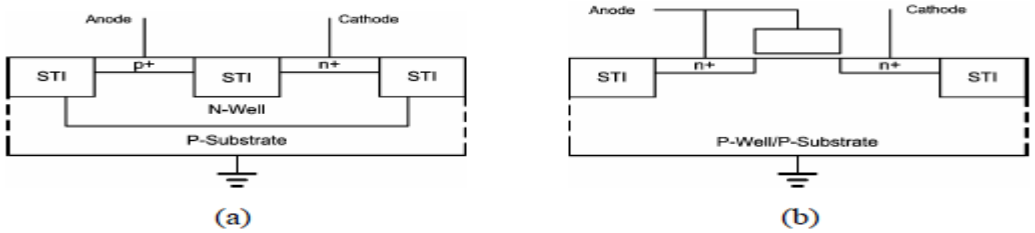

Figure 1. Schematic cross sections of (a) the p+/n-well diode, and (b) the diode-connected NMOS, in grounded p-type substrate. [1]

In this paper, an on-chip high-voltage charge pump circuit is proposed with the polysilicon diodes . Because the anode and the cathode of the polysilicon diode is fully isolated from the substrate, the voltage on the anode or the cathode of the polysilicon diode is not limited by the breakdown voltage of the undesired pn-junction.

II. POLYSILICON DIODES

A. Structure : In the previous processes, the gates of PMOS and NMOS are both realized with the n-doped polysilicon. Because of the work function consideration, the gate of PMOS and the gate of NMOS are realized with the p-doped polysilicon and the n-doped polysilicon , respectively. In order to make the different types of polysilicon gates, the intrinsic polysilicon layer is deposited first, and then the p-type and n-type impurities are doped into the intrinsic polysilicon to form the gate and the NMOS gate accordingly . So, the diode can be realized on the polysilicon layer by recent process. Figure 2 shows the cross section of the polysilicon diode in the standard CMOS process. As depicted in Figure , the STI (shallow trench isolation) layer is located above the silicon bulk. The polysilicon layer is deposited above the STI layer. Then, the p-type and n-type highly doped regions on the polysilicon are doped with the same process for the PMOS and NMOS source/drain implementation, respectively. As the polysilicon diode is formed on the STI layer, it is isolated from the silicon bulk. Thus, the charges on the anode and the cathode of the polysilicon diode dosen't leak to the silicon substrate. In the this diode, an extra un-doped polysilicon region can be inserted between the p-type and n-type doped polysilicon regions. The length (Lc) of the un-doped center region could be used to adjust the I-V characteristics of the polysilicon diode.

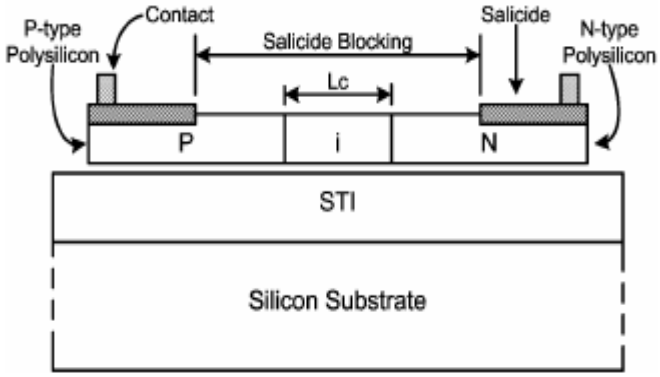

Figure 2. Schematic cross section of the polysilicon diode in the standard (bulk) CMOS process.[1]

B. Characteristics of Diodes realized : The polysilicon diodes with different lengths (Lc) of the un-doped center region had been fabricated in a 0.25-μm 2.5-V standard CMOS process, where the Lc is changed from 0.25 μm to 1.5 μm [1]. Figure 3 depicts the measured I-V curves of the polysilicon diodes with different Lc. Figure 4 depicts the measured cut-in voltages of the polysilicon diodes with different Lc, where the cut-in voltages are defined at the 1-μA forward biased current. In Figure 4, the cut-in voltages of polysilicon diodes vary from 0.47 V to 0.58 V. As the length of the un-doped region increases beyond 0.9 μm, the cut-in voltage saturates at around 0.58 V.

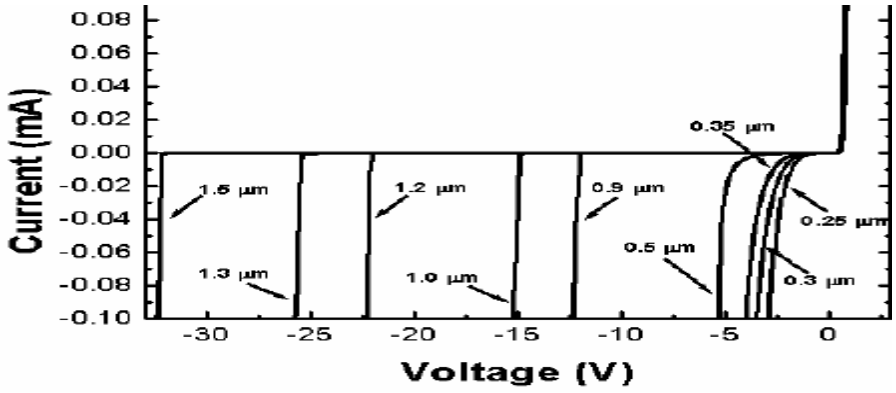

Figure 3. Measured I-V curves of the polysilicon diodes with different lengths (Lc) of the un-doped center region.[1]

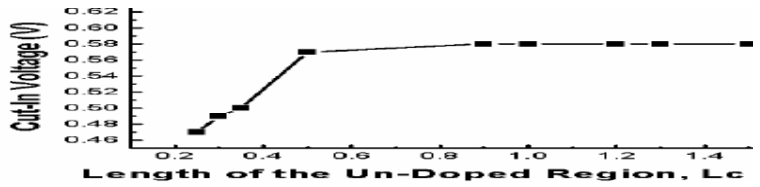

Figure 4. Measured cut-in voltages of the polysilicon diodes with different lengths of the un-doped center region. The cut-in voltages are defined at the 1-μA forward biased current.[1]

Figure 5 depicts the measured reverse breakdown voltage of the polysilicon diode with different Lc, where the reverse breakdown voltage is defined at the 1-μA reverse biased current. This shows the reverse breakdown voltage increases when the Lc increases. As the Lc is greater than 1.2 μm, the reverse breakdown voltage goes beyond 20 V.The reverse breakdown voltage is 33 V when the length of the un-doped region is 1.5 μm. Thus, the reverse breakdown voltage of the polysilicon diode can be adjusted by changing the length of the un-doped center region .

III. POLYSILICON DIODES IN CHARGE PUMP CIRCUIT

Figure 6 depicts the 4-stage charge pump circuit designed with polysilicon diodes (D1~D5), and the clock signals CLK and CLKB are out-of-phase and with the amplitude of VDD (2.5 V). The RL and CL represent the output loading of resistance and capacitance, respectively. The CL makes the output voltage more stable. If the parasitic capacitance at each node and the output current through the RL can be ignored, the ideal output voltage of the charge pump circuit is expressed as

$$Vout = (n + 1) \times (VDD – VD), \qquad (1)$$

here VD is the cut-in voltage of the polysilicon diode and n is the number of stages in the circuit. Thus, as the number of stages increases, the output voltage of the charge pump circuit can also be increased.

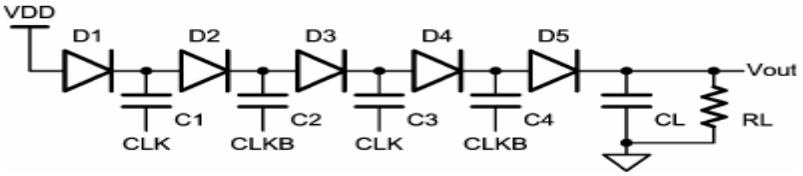

Figure 6. 4-stage charge pump circuit realized with 5 polysilicon diodes.[1]

IV. CONCEPTUAL RESULTS

Figure 7 depicts the measured output voltages of the 4-stage, 8-stage, and 12-stage charge pumpcircuit with the polysilicon diode having 0.5-μm or 1-μm un-doped center region (Lc). As depicted in Figure 7, the measured output voltages of the charge pump circuit with the polysilicon diodes (Lc=0.5 or 1 μm) are almost the same. The length of the un-doped region (Lc) doesn't obviously affect the output voltage of the charge pump circuit because the voltage across each polysilicon diode not exceed VDD (2.5 V), which is less than the reverse breakdown voltages of the polysilicon diodes (Lc=0.5 or 1 μm). Figure 8 depicts the measured output voltages of the 4-stage, 8-stage, and 12-stage charge pump circuits with the polysilicon diodes (Lc=1 μm) to drive output resistors (RL). If the RL is high , the output current is small. As depicted in Figure 8, the output voltage degrades when the RL is decreased .

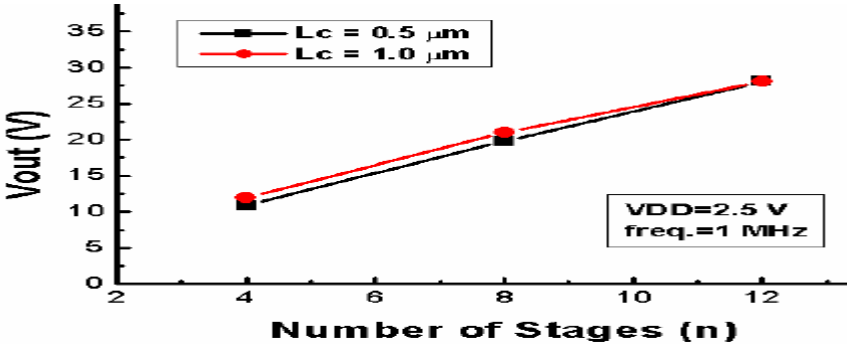

Figure 7. Measured output voltages of the 4-stage, 8-stage, and 12-stage charge pump circuits with the polysilicon diodes having 0.5-μm and 1-μm un-doped region to drive capacitive load. The clock frequency is 1 MHz and the power supply voltage (VDD) is 2.5 V.[1]

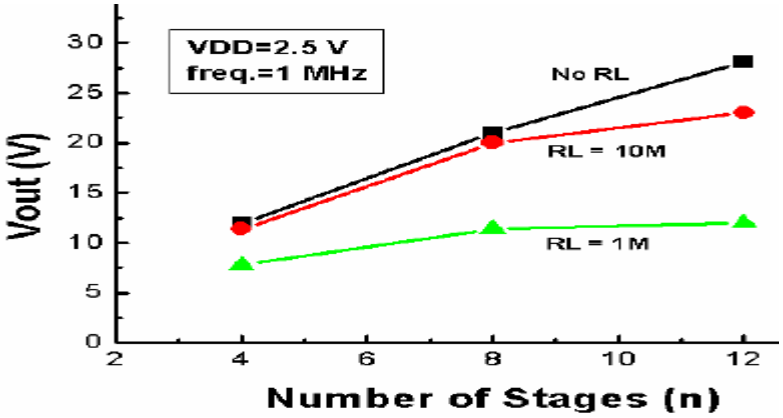

Figure 10. Measured output voltages of the 4-stage, 8-stage, and 12-stage charge pump circuits (Lc=1 μm) with the output loading of 1 MΩ, 10 MΩ, or without the output resistor. The clock frequency is 1 MHz and the power supply voltage (VDD) is 2.5 V.[1]

V. CONCLUSION

On-chip high-voltage charge pump circuit realized with the polysilicon diode had successfully verified in a standard (bulk) CMOS process. The polysilicon diode is formed on the STI layer, which is isolated from the bulk. Thus, the output voltage of the charge pump circuit with the polysilicon diodes is not limited by the junction breakdown voltage. The 4- stage, 8-stage, and 12-stage charge pump circuit with 10-pF on-chip pumping capacitors and the polysilicon diode having 0.5-μm and 1-μm un-doped center region had been fabricated in a 0.25-μm 2.5-V standard (bulk) CMOS process. To drive the capacitive load, measured result shows that the 12-stage charge pump circuit with the polysilicon diodes (Lc=0.5 μm) can pump the output voltage as high as 28.08 V. The loading effect is measured in this work. Thus ,By using this polysilicon diodes, the negative charge pump circuit can be also implemented in the standard CMOS processes without the limitation of the junctions.

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