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Comparative Analysis of low area and low power D Flip-Flop for Different Logic Values

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----------ABSTRACT----------
In this paper we propose to increase the performance of flip flops a set of rule for consistent estimation of the performance and power features of the flip flop. A new simulation and optimization approach is presented triggering both high performance and power budget issue . The analysis approach revels the source of performance and power consumption bottlenecks in different design styles. Certain misleading parameters have been properly modified and the flip flop analysis on the bases of performance

KEYWORDS:- *flip flops, optimization approach, power consumption bottlenecks*

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I. INTRODUCTION

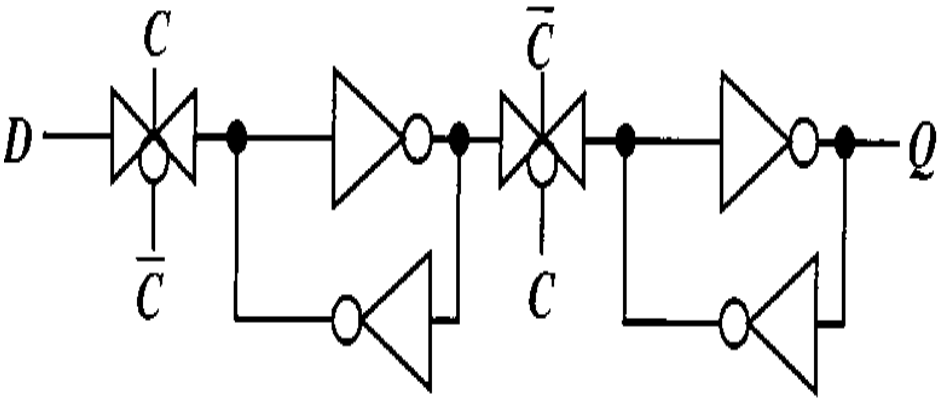
With an increasing demand for higher performance and lower power dissipation in current microprocessor, new circuit design techniques are needed for both switching logic and storage devices. In a digital system, flip-flops are often thought of as memory devices, whose primary function is to store state information and data results. *As* complexity in microprocessor increases, both logic requirements and storage depth Swill also increase. This will lead to a larger number of flip-flops and may result in larger power consumption. In fact, the maximum speed of a flip-flop is directly proportional to the total power dissipated. In the mobile part used in today's computer notebooks, emphasis on power dissipation has been a major primarily design concern.

One way for a system to save power is to enter a sleep mode where the states of the logic remain saved until the system becomes active again. This is achieved by turning off the clock and forcing the system into a standby state. Once the system enters this state, the storage
capacitance may leak over time resulting in a loss of stored information. To maintain the capacitive charge during sleep mode, a positive feedback inverter or level restorer is required. Such configurations are considered to be a pseudo-static design; a dynamic CMOS latch with feedback that refreshes itself to retain the stored content. The high gain from the cross-coupling inverter makes pseudo-static flip-flop ideally as signal driver. When the system revives into its normal state, the control logic reinitializes and continues where it last left off.

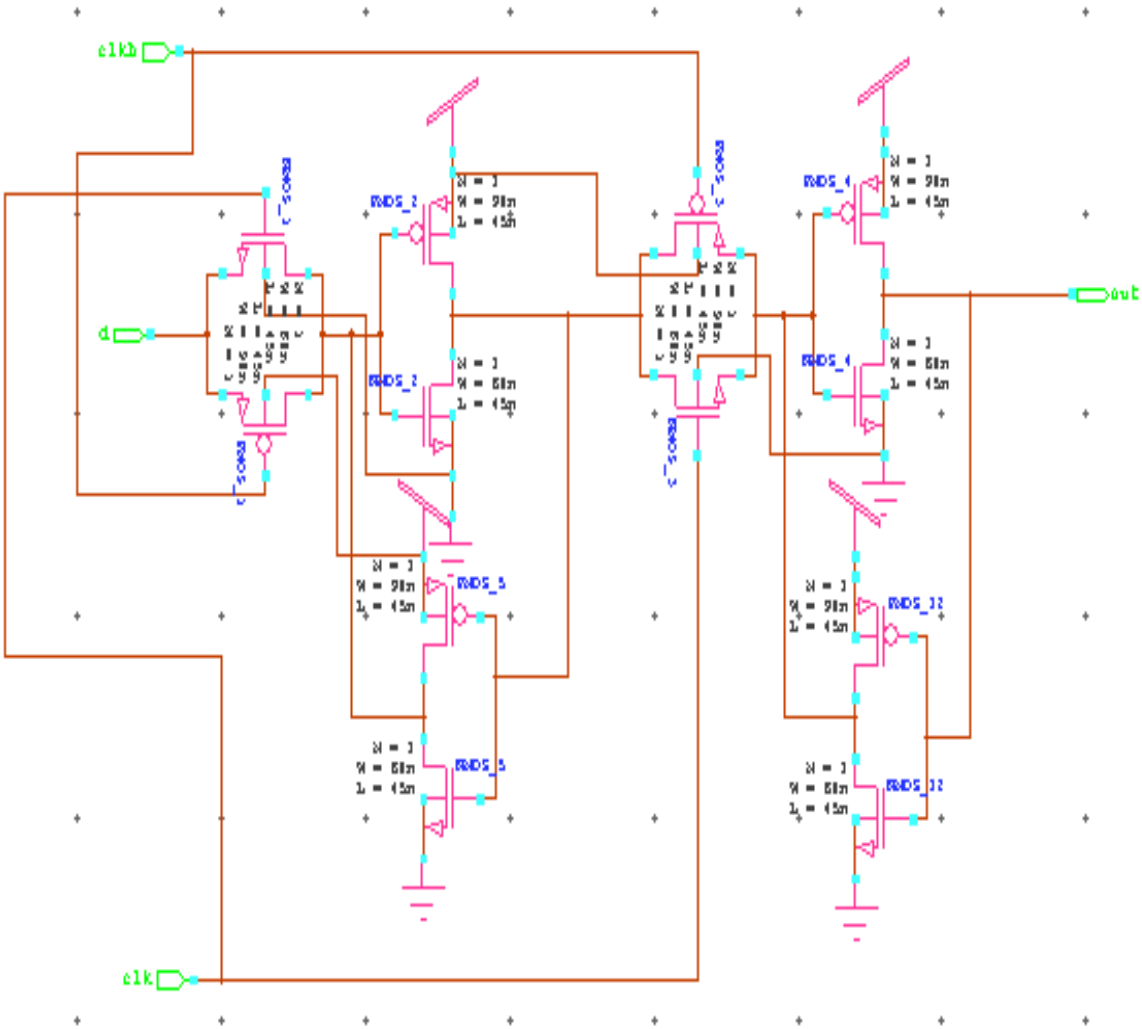
II. ANALYSIS AND SIMULATION

3.3.2 Low Area D-FF

A common approach for reducing area overhead of the conventional DFF is to remove the two feedback transmission gates. This low-area DFF is depicted in Fig. 1(b). Although the strength of feedback inverters has been weakened to minimize short-circuit power dissipation due to voltage contention, this low-area DFF still consumes 18% more total power and is 42% slower (or has 76% more energy) compared to the conventional DFF.



Schematic of low power D-FF



schematic of low area D-flip-flop using tanner tool

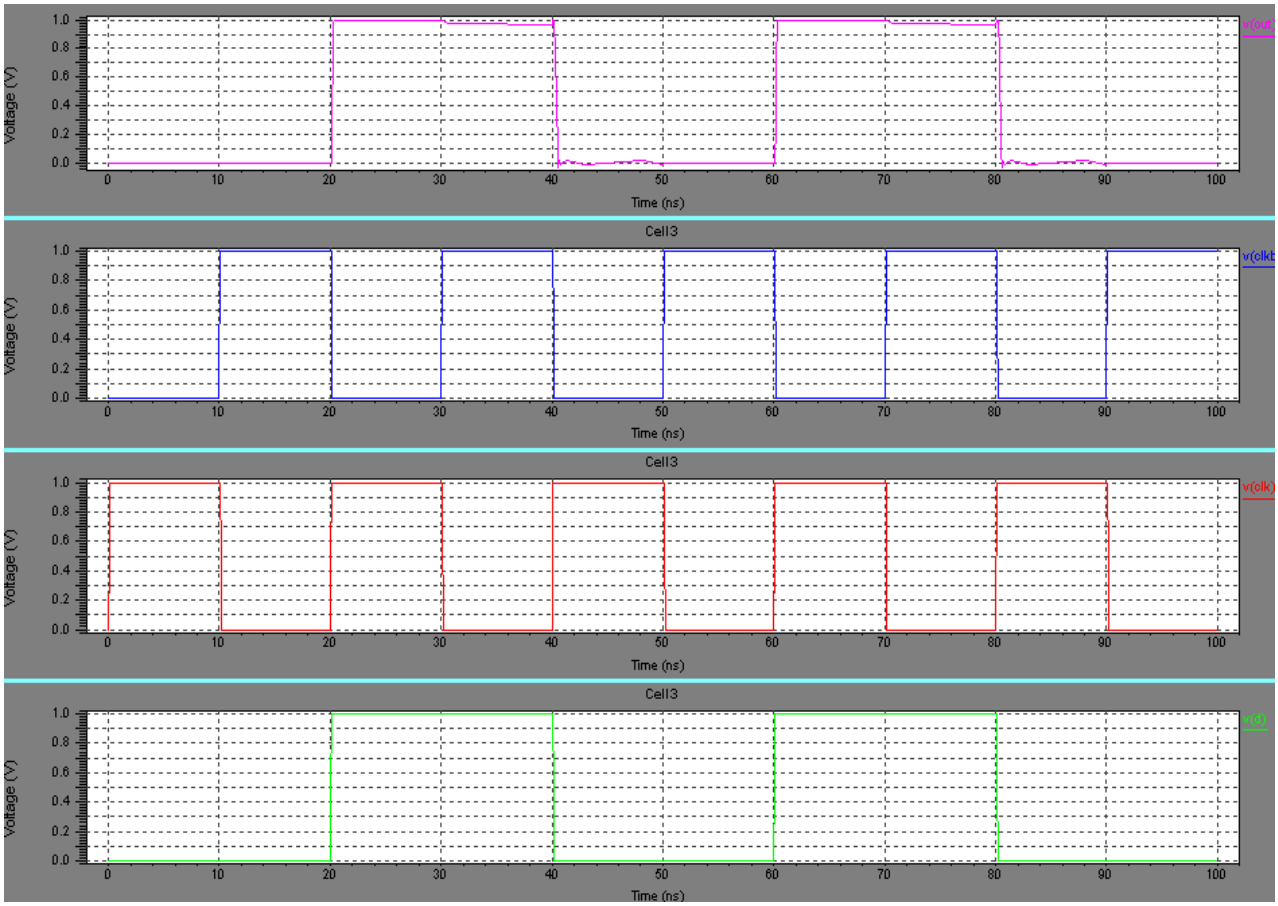


Figure Simulation result of low area D flip flop

Low-Power D-FF

One approach to optimize for power dissipation is to replace the inverter and transmission gate in the feedback path of conventional D-FF with a single tri-state inverter. This approach is referred to as a low-power DFF.

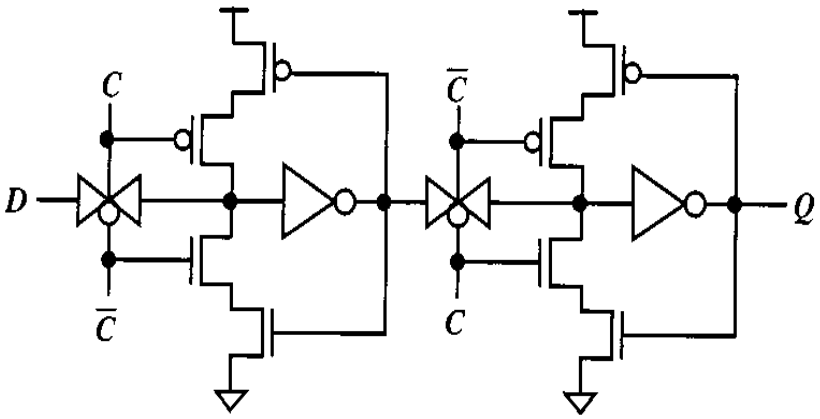
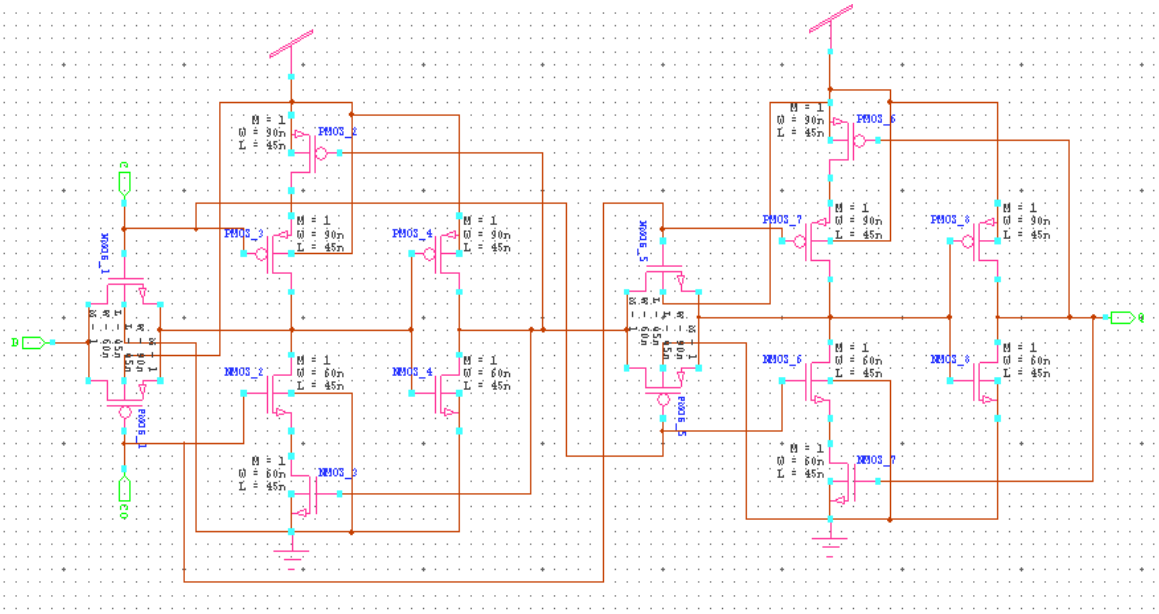
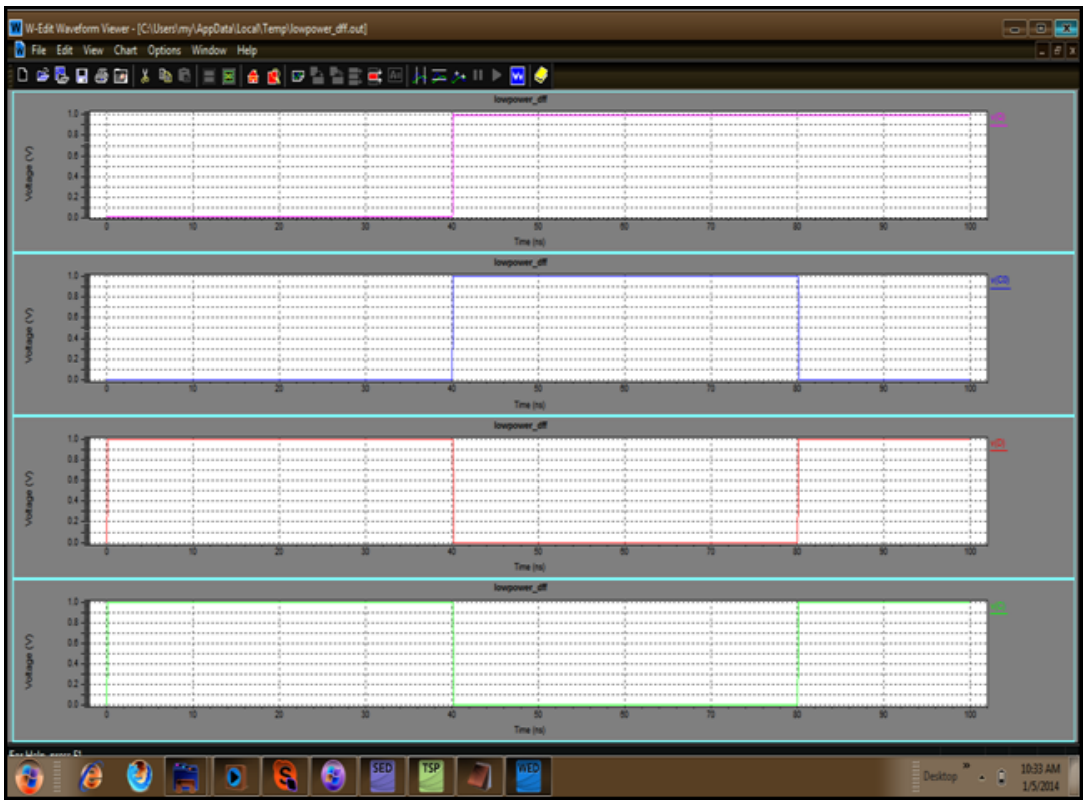


Fig. 3.5 Schematic of low power D-FF



Schematic of Low Power D-FF using Tanner tool



Simulation result of low power D flip flop

III. RESULTS & DISCUSSION

In this thesis various types of D-FF are designed and simulated using TANNER tool. The Simulation results in the tables given below. Tanner 14.1 tool schematic editor is used to draw schematic of the D-FF. Schematic of these flip-flops are firstly designed on tanner's schematic editor and net lists of the circuits are than taken out. These net lists run with 45 nm Predictive Technology Model (PTM) file on tanner's spice simulator to get simulation results. Various D-flip flops are designed and simulated on different power supply like 0.8V ,1 V and 1.2 V and than their results has been compared on the basis of number of transistors, power consumption and Delay

Power analysis of Low power D flip flop is as

Supply voltage	0.8 V	1.0 V	1.2V
Power (N-watt)	0.71	1.042	1.14

Power analysis of low area D flip flop is as

Supply voltage	0.8 V	1.0 V	1.2V
Power (N-watt)	1.57	1.69	1.719

Delay analysis of Low power D flip flop is as

Supply voltage	0.8 V	1.0 V	1.2V
Delay (N-Sec.)	2.001	2.0035	2.0050

Delay analysis of Low Area D flip flop is as

Supply voltage	0.8 V	1.0 V	1.2V
Delay (N-Sec.)	1.816	1.808	1.7911

IV. CONCLUSION

Sequential circuits required different types of memory elements some of them required fast speed and some of them required low power and low area thus in this work a comparative analysis of different D flip flop is done which concluded that some D flip flop is fastest in speed and someone consumes less power for designing optimized value of PDP (power delay product) has been calculated.

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