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Design of Xilinx (8.1) FPGA Based Five Level (Multilevel) PWM Single Phase Inverter

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----------ABSTRACT----------

In this paper a Xilinx 8.1 FPGA Based Five Level PWM Single Phase Inverter was constructed by control and power circuit with addition of MOSFETS and in bridge topology and VLSI programming used for the generation PWM pulses. The inverter can produce five different output voltage levels across the load. Xilinx FPGA is a programmable logic device developed by Xilinx 8.1 which is considered as an efficient hardware for rapid prototyping. It is used as a PWM generator to apply the appropriate signals to the inverter switches. In addition to Xilinx FPGA software was used for simulation and verification of the proposed circuit before implementation. Simulation and experimental results show that both are in close agreement.

KEYWORDS *– Modulation index, PWM, System Clock, Harmonics*

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I. INTRODUCTION

Multilevel inverters have been attracting as power converters of choice in many applications. They have significant advantages over the conventional one because of the capability to reduce the undesirable harmonics in order to improve the performance and efficiency. Waveform synthesis methods for these inverters include

1) Staircase modulation
2) Sine-triangle carrier modulation
3) Space vector modulation

Normally the topological structure of multilevel inverter suggested must cope with the following points.

1) It should have less switching devices as far as possible
2) It should be capable of enduring very high input voltage such as HVDC transmission for high power applications
3) Each switching device should have lower switching frequency.

PWM generation is more important in the inverter design and Several multicarrier techniques have been developed to reduce the distortion in multilevel inverters, based on the classical (SPWM) with triangular carriers.

Xilinx field programmable gate arrays (FPGA's) are standard integrated circuits that can be programmed by a user to perform a variety of logic functions. Xilinx FPGA enables to produce prototype logic designs right in a short period. It is possible to create, implement, and verify a new design. The FPGA architecture consists of three types of configurable elements - a perimeter of input/output blocks (IOBs), a core array of configurable logic block (CLBs), and resources for interconnection. The IOBs provide a programmable interface between the internal array of logic blocks (CLBs) and the device's external package pins. CLBs perform user-specified logic functions, and the interconnect resources.[6], [7]

II. FPGA BASED FIVE LEVEL PWM INVERTER

2.1 System Overview

In this project a combination of software and hardware that is FPGA chip and VHDL language is used to generate the PWM pulses. The programming is done in such a way that the mode of operation of inverter is 180 degree. We have implemented driver circuit, inverter control card using power circuit (using MOSFETs) as per our traditional way of design.

The project is implemented using Spartan-II chip (FPGA chip), which is a large capacity chip. (Logic cells-1728 & system gates-50000) so that future modifications and developments can also be incorporated. The code

tends to be secret. Since once it is coded in FPGA chip, it is not readable. The software used in the project where:
1) Modelsim for simulation.
2) Xilinx for design entry and downloading to the kit.
Along with the power circuitry one also requires VLSI hardware (i.e. the downloading kit and FPGA chip) in which one can download the VHDL code.

2.2 Block Diagram of System

The system is divided into following two main parts. The system diagram is shown in fig. 2.1
1) Control circuit
2) Power circuit or bridge circuit

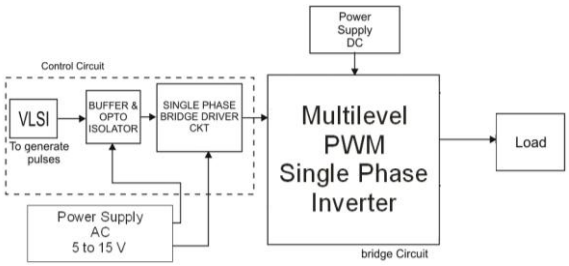

Figure 2.1 : Block diagram of five level PWM single phase inverter

2.2.1 Control Circuit

Control circuit is divided into following three parts. Which is given below.
a) VLSI, b) buffer and optoisolator, c) single phase bridge driver circuit.
The control circuit is also needs power supply of +5V and +15V DC.

a) VLSI Block (to generate pulses)

This is a combination of hardware and software. The programme was written using VHDL language. The four pin switch (i.e. readmode index) is provided to change the width of the pulses. It is important part of VHDL code because as per the requirements of user this controls single phase power. In the programme two changes are used to generate the pulses; those are readmode index and mode selection. The power of the system can be changed by changing the readmode index .This programme is downloaded on FPGA chip to generate the PWM pulses required to drive the power circuit.

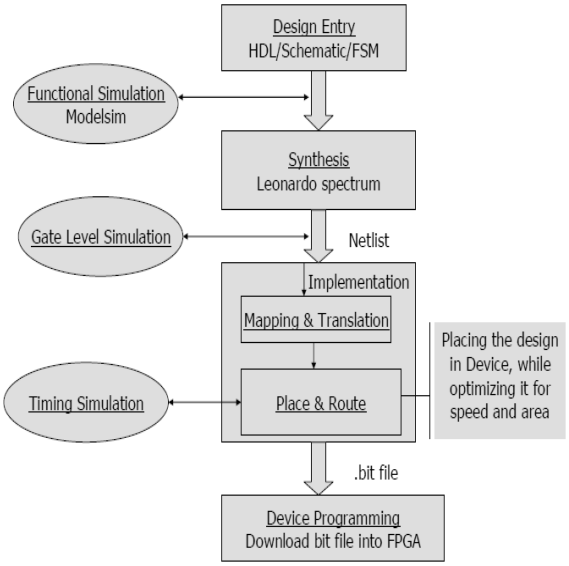

Figure 2.2 : Flowchart for software implementation

b) Buffer and optoisolator

The generated pulses are given to the buffer and optoisolator circuit 74LS245 bidirectional buffer is used. The buffer takes the pulses from FPGA chip and passes them to six optoisolators (PC817). Optoisolator

(PC817) are used to isolate the VLSI part from the power circuit. The pulses coming from optoisolator are given to the sing phase driver circuit.

c) Single phase bridge driver circuit

For the single phase bridge driver circuit IR2130 (i.e. driver IC) is used. The driver IC drives the power circuit. The pulses are given to the power circuit through driver circuit. This IC is used for short circuit protection etc.

2.2.2 Power or Bridge Circuit

The power or bridge circuit consists of two switches S5 and S6 and four diodes are added to the conventional full-bridge inverter.

The function of bi-directional switch is to control current flow. The PWM pattern adopted in the proposed inverter makes the inverter producing output voltage with three levels (zero and half supply dc voltage positive and negative respectively) at modulation index (Ma $\leq$ 0.5) and five levels (zero, half and full supply voltage positive and negative respectively) at modulation index (Ma > 0.5).

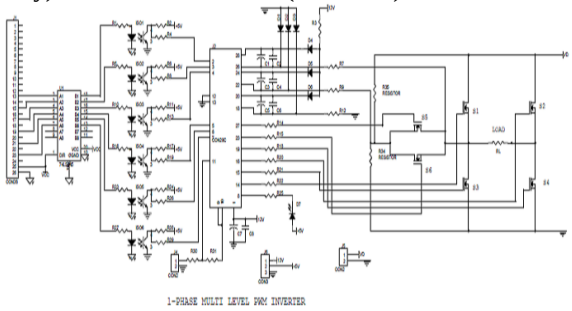

Figure 2.3 : Proposed power or bridge circuit

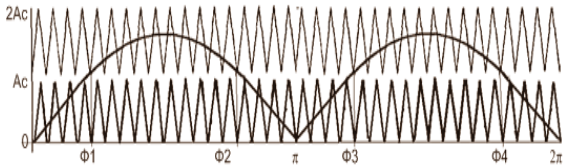

Figure 2.4 : PWM Generation Techniques used for the Multilevel PWM Single Phase Inverter

The modulation process is defined as follows.

1) The modulation index is defined as:

$$Ma = \frac{Am}{2\,Ac} \qquad (1)$$

Where Am is peak value of sinusoidal wave
Ac is the peak value of carrier wave

2) The frequency modulation index

$$Mf = fc/fm \qquad (2)$$

Where *fc* is the frequency of the carrier wave
fm is the frequency of the sinusoidal wave.

3) The angle of displacement existing between the sinusoidal wave and the first positive carrier wave can be defined as following

Am.Sin (□1) = Ac

$$\alpha 1 = \sin^{-1}\left(\frac{Ac}{Am}\right) \quad (3)$$

$$\alpha 2 = \pi - \alpha 1 \quad (4)$$

$$\alpha 3 = \pi + \alpha 1 \quad (5)$$

$$\alpha 4 = 2\pi - \alpha 1 \quad (6)$$

The proposed inverter may be operate in four modes defined as following

Mode 1: $\alpha 1 < wt < \alpha 2$ (7)

Mode 2: $0 < wt \leq \alpha 1$ and $\alpha 2 < wt \leq \pi$ (8)

Mode 3: $\pi < wt \leq \alpha 3$ and $\alpha 4 < wt \leq 2\pi$ (9)

Mode 4: $\alpha 3 < wt \leq \alpha 4$ (10)

At modulation index Ma > 0.5 the inverter operates in all modes producing five voltage levels 0, Vdc/2,Vdc, -Vdc/2, -Vdc respectively.

At certain load when the required voltage is Vdc/2 or less the inverter operates at modulation index Ma≤0.5 in two modes 2 and 3 only. The displacement angles become [7].

$$\alpha 1 = \alpha 2 = \frac{\pi}{2} \quad (11)$$

$$\alpha 3 = \alpha 4 = \frac{3\pi}{2} \quad (12)$$

Table 2.1 Output Voltage Based on Switches Combination[7]

On Switches	Va	Vb	Vab=Vo
S4,S1	Vdc	0	+Vdc
S4,S6	Vdc/2	0	+Vdc/2
S4,S3	0	0	0
S2,S1	Vdc/2	Vdc/2	0
S2, S5	0	Vdc	-Vdc
S2,S3	0	Vdc/2	-Vdc/2

III. THE PWM GENERATION USING XILINX FPGA

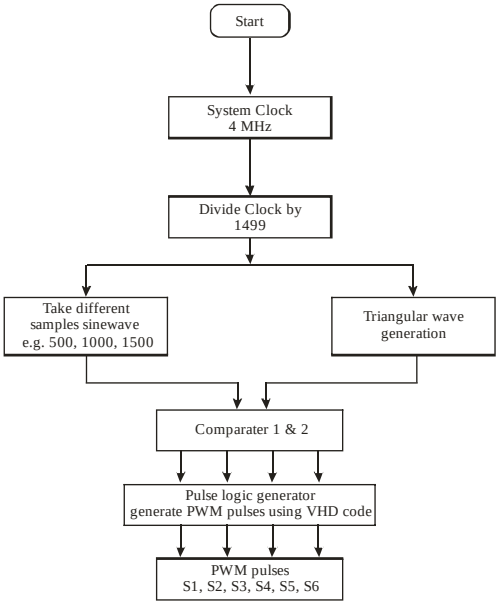

Figure 3.1 : PWM pulse generation flowchart

The system clock frequency is 4 MHz. divide the system clock frequency by clock divider 1499 and 50. Different samples for sinewave are taken e.g. 500, 1000, 1500. For triangular wave generation up down counter is used and VHDL programme includes sample addition process is also writer and converted into schematic blocks (addition unit) to generate two types of carrier (upper and lower) waves. The main clock frequency is determined by the following formula.

$fclk = fc\ (2^n - 1)$

Where *fclk* is the main clock frequency, *fc* is the carrier (upper and lower) wave frequencies and *n* is the bit size of the up-down counter.

Comparator compare the sinewave and triangular wave and finally generate the PWM pulses using VHDL code.

IV. SIMULATION AND EXPERIMENTAL RESULTS

Simulation is functional emulation of a circuit design through software programmes that use models to replicate how waveforms will perform in terms of timing and results or is the process of applying stimuli to model overtime and producing corresponding responses from model at stimulated time when those responses would occur. Simulation eliminating the time consuming need for constant physical prototyping. Simulation can be performed during all stages of design.

The simulation results of all components used in the design is done to check the functionality. Waveforms shows the six pulse getting signal output for different switch positions shown in Fig. 4.1.

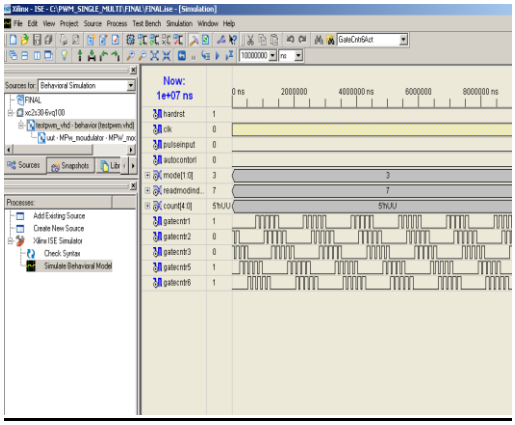

Figure 4.1 : Software simulation results with different read mode index

Figure 4.2 : Five level inverter output photograph across load

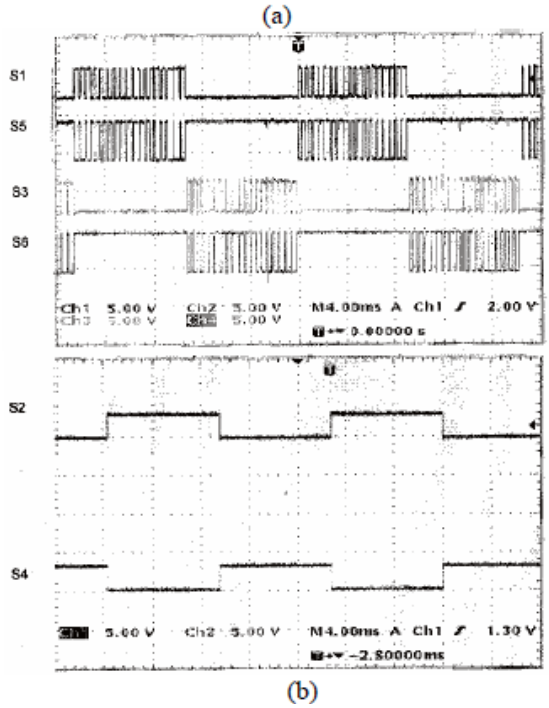

Figure 4.3 : Multilevel single phase PWM at Ma = 0.4
(a) Simulated (b) Experimental

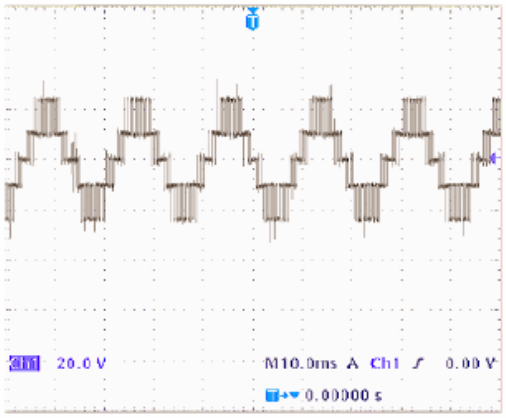

Figure 4.4 : Unfiltered output voltage five levels at Ma = 0.8

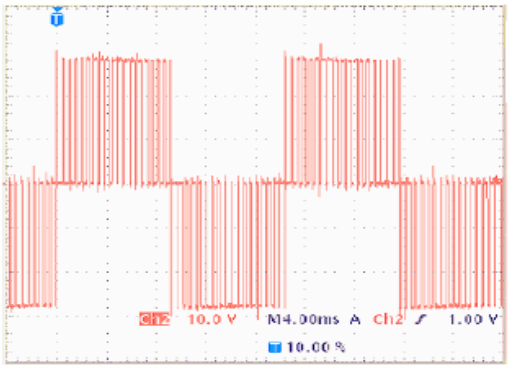

Figure 4.5 : Unfiltered output voltage three levels at Ma = 0.4

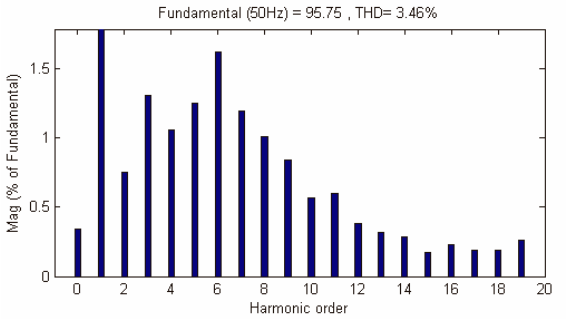

Figure 4.6 : Harmonic order Ac voltage across the load

V. CONCLUSION

The PWM switching patterns were applied to the proposed inverter to produce five level output voltage. Xilinx FPGA C2530VQ100 is enable fast with bit file, flexible design and implementation is done. The simulation and experimental results were satisfactory for pulse generation, five level output voltage and the readings are taken for output voltage and current. Thus it is converting the AC output from DC input.

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