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Restoring the Power Quality by Combined Shunt and Series Compensation in Power Transmission Lines

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----------Abstract----------

The main objective of this paper is to develop a novel reference signal generation method for the unified power quality conditioner (UPQC) adopted to compensate current and voltage-quality problems of sensitive loads. The UPQC consists of a shunt and series converter having a common dc link. The shunt converter eliminates current harmonics originating from the nonlinear load side and the series converter mitigates voltage sag/swell originating from the supply side. The developed controllers for shunt and series converters are based on an enhanced phase-locked loop and nonlinear adaptive filter. The dc link control strategy is based on the fuzzy-logic controller. A fast sag/swell detection method is also presented. The efficacy of the proposed system is tested through simulation studies using the Power System Computer Aided Design/Electromagnetic Transients dc analysis program. The proposed UPQC achieves superior capability of mitigating the effects of voltage sag/swell and suppressing the load current harmonics under distorted supply conditions.

Keywords: Active filter, custom power, fuzzy-logic controller, reference signal generation, unified power-quality conditioner (UPQC)

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I. Introduction

The electric power system is considered to be composed of three functional blocks - generation, transmission and distribution. For a reliable power system, the generation unit must produce adequate power to meet customer's demand, transmission systems must transport bulk power over long distances without overloading or jeopardizing system stability and distribution systems must deliver electric power to each customer's premises from bulk power systems. Distribution system locates the end of power system and is connected to the customer directly; to the power quality mainly depends on distribution system. The reason behind this is that the electrical distribution network failures account for about 90% of the average customer interruptions. In the earlier days, the major focus for power system reliability was on generation and transmission only as these more capital cost is involved in these. In addition their insufficiency can cause widespread catastrophic consequences for both society and its environment. But now a day's distribution systems have begun to receive more attention for reliability assessment.

Initially for the improvement of power quality or reliability of the system FACTS devices like static synchronous compensator (STATCOM), static synchronous series compensator (SSSC), interline power flow controller (IPFC), and unified power flow controller (UPFC) etc are introduced. These FACTS devices are designed for the transmission system. But now a day more attention is on the distribution system for the improvement of power quality, these devices are modified and known as custom power devices. The main custom power devices which are used in distribution system for power quality improvement are distribution static synchronous compensator (DSTATCOM), dynamic voltage Restorer (DVR), active filter (AF), unified power quality conditioner (UPQC) etc. In this thesis work from the above custom power devices, DVR is used with PI controller for the power quality improvement in the distribution system. Here two different loads are considered, one is linear load and the other is induction motor. Different fault conditions are considered with these loads to analyze the operation of DVR to improve the power quality in distribution system

II. Related work

From the literature review, it is observed that the work on the investigation on power with compensating devices is very much diversified. However it is observed that there is a scope to investigate the effectiveness of compensating devices for different loads and with different loading conditions in distribution system. As the distribution system locates the end of power system and is connected to the customer directly, so the reliability of power supply mainly depends on distribution system. As the customer's demand for the reliability of power supply is increasing day by day, so the reliability of the distribution system has to be increased. Electrical distribution network failures account for about 90% of the average customer interruptions. So it is highly required to increase the reliability of the distribution system. The objective of the proposed work is to improve the power quality or reliability in the distribution system with the use of custom power device. Different fault conditions are considered with different loads to analyze the operation of UPQC for the improvement the power quality in distribution system.

2.1 Proposed UPQC

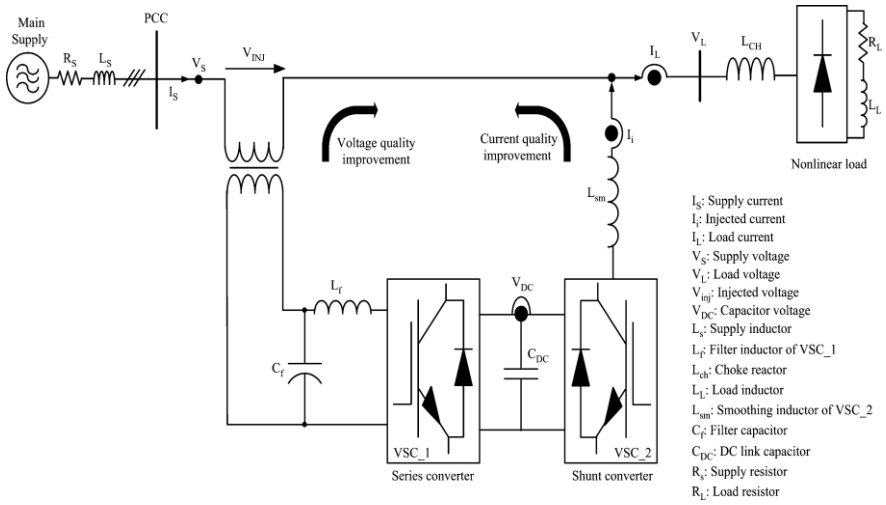

Fig 2.1 Schematic diagram of UPQC.

Power quality issues are becoming more and more significant in these days because of the increasing number of power electronic devices that behave as nonlinear loads. A wide diversity of solutions to power quality problems is available for both the distribution network operator and the end user. UPQC has attracted the attention of power engineers to develop dynamic and adjustable solutions to PQ problems.

2.2 Power Circuit Configuration

UPQC consists of two VSC's that are connected back to back through a common energy storage DC capacitor (Cdc). Series converter (VSC1) is connected through transformers between the supply and point of common coupling (PCC). Shunt converter (VSC2) is connected in parallel with PCC through the transformers.

VSC1 operates as a voltage source while VSC2 operates as a current source. The power circuit of VSC1 consists of three single- phase H-bridge voltage source PWM inverters. H-bridge inverters are controlled independently. The main objective of VSC1 is to mitigate voltage sag / swells from supply side. The power circuit of VSC2 consisting of three- phase voltage source PWM inverter is supplied from Cdc. VSC2 is directly connected through a boost inductor Lsm which can boost up the common Dc link voltage to the desired level. The main objectives of VSC2 are to regulate the Dc link voltage between both converters and to suppress the load current harmonics.

2.3 Energy Storage Unit

DC link (energy storage unit) supplies required power for compensation of load voltage during voltage sag / swell or current harmonics. UPQC generally consists of two voltage converters (series and shunt) using IGBT which operate from a common Dc link storage capacitor.

2.4 LC Filter

The effect of harmonics generated by the inverter can be minimized using inverter side and line side filtering. Inverter side filtering scheme has the advantage of being closer to harmonic source thus high order harmonic currents are prevented to penetrate into series injection transformer but this scheme has the advantages of causing voltage drop and phase angle shift in the fundamental component of the inverter output. In line side filtering scheme, harmonic currents penetrate into series injection transformer but voltage drops and phase shift problems do not disturb the system. Inverter side LC filtering is generally preferred for both series sides and inverter side L filtering is preferred for shunt side.

2.5 Injection Transformer

Series converter of UPQC is most of time in standby mode and conduction losses will account for the bulk of converter losses during the operation. In this mode the series injection transformer works like a secondary shorted current transformer using bypass switches delivering utility power directly to the load

III. Control Unit Of Upqc

The control unit is the most important part of the UPQC system. Rapid detection of disturbance signal with high accuracy, fast processing of the reference signal and high dynamic response of the controller are the prime requirements for desired compensations. The main considerations for the control system of UPQC include:

- Series converter control
- Shunt converter control

3.1 Series Converter Control

The series converter control includes the reference voltage and sag/swell detection computations. Fig3.1 shows the control algorithm of a series converter for Phase A. This control algorithm identical for other phases.

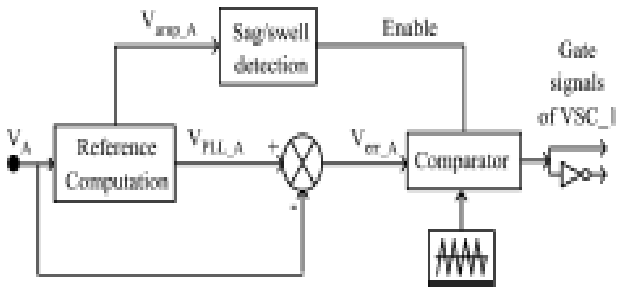

Fig 3.1 : Control block diagram of series converter.

3.1.1. Reference Voltage Generation

A block diagram of the proposed algorithm is shown in Fig.3.2. The proposed controller algorithm is derived from the findings of both enhanced PLL and nonlinear adaptive filter. The proposed controller minimizes the mathematical operands in the system and reduces complex parameter tuning. The measurements of supply voltages are required for the control strategy of VSC_1.The system receives the measured input signal and provides an online estimate of the following signals:

1) B(t), the difference of input and the synchronized fundamental component;
2) C(t) , the amplitude of D(t) ;
3) D(t) , the synchronized fundamental component;

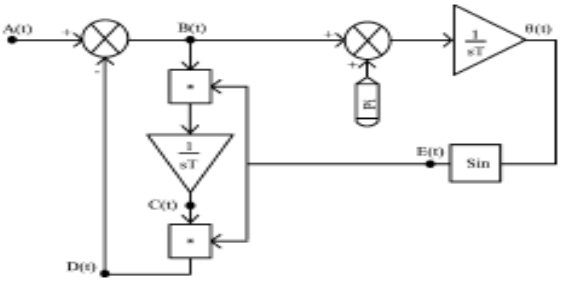

Fig 3.1.1: Block diagram of the proposed algorithm

4) E(t) , PLL signal;
5) Θ(t) , the phase angle of D(t).

The control signals of the proposed controller are derived from the following equations.
B(t)can be expressed as a continuous time

$$B(t) = A(t) - E(t)\int B(t)E(t)dt \quad (1)$$

In (1),B(t) and E(t) , located at the right-hand side of (1),are assumed as a constant due to the value at the instant t that is equal to that of the instance(t-1) . Hence, the final statement of (1) is given in

$$B(t) = A(t) - E(t-1)\int B(t-1)E(t-1)dt \quad (2)$$

Considering that B(t-1) and E(t-1) are constant, then

$$B(t) = A(t) - B(t-1)E^2(t-1)\int dt \quad (3)$$

If the constants are assumed as

$$B(t-1)E^2(t-1) = k_1 \quad (4)$$

Then the last statement of B(t) can be written as

$$B(t) = A(t) - k_1 t \quad (5)$$

Θ(t) can be expressed as

$$\theta(t) = \int (B(t) + \pi)dt \quad (6)$$

Substituting B(t) and A(t)= A sin ωt into Θ(t). then

$$\theta(t) = \int ((A\sin\omega t - k_1 t) + \pi)dt \quad (7)$$

The last statement of Θ(t) is given in

$$\theta(t) = -\frac{A}{\omega}\cos\omega t - \frac{k_1}{2}t^2 + \pi t \quad (8)$$

E(t) can be expressed as

$$E(t) = \sin\theta(t) \quad (9)$$

Substituting Θ (t) into the E(t), E(t) can be written as

$$E(t) = \sin(-\frac{A}{\omega}\cos\omega t - \frac{k_1}{2}t^2 + \pi t) \quad (10)$$

C(t) can be expressed as

$$C(t) = \int B(t)E(t)dt \quad (11)$$

In (11),E(t) is assumed as a constant due to the value at the instant t which is equal to that of the instance(t-1) . Hence, the last statement of (11) is given in the following text:

$$C(t) = \int B(t)E(t-1)dt \quad (12)$$

Considering that $E(t-1) = k_2$ is a constant, then

$$C(t) = k_2\int (B(t)dt) \quad (13)$$

Substituting B(t) into C(t), C(t) can be expressed as

$$C(t) = k_2\int (A\sin\omega t - k_1 t)dt \quad (14)$$

The last statement of C(t) can be written as follows:

$$C(t) = \frac{-k_2 A}{\omega}\cos\omega t - \frac{k_1 k_2}{2}t^2 \quad (15)$$

C(t)can be expressed as

$$D(t) = C(t) * E(t) \quad (16)$$

$$D(t) = C(t)\sin\theta(t) \quad (17)$$

The last statement of D(t) can be written as follows:

$$D(t) = C(t)\sin(\frac{Ct}{k_2} + \pi t) \quad (18)$$

Diagram shows the supply voltage and its extracted components, such as the difference of input and the synchronized fundamental component B(t) , the amplitude C(t) , synchronized fundamental component D(t) , and PLL signal E(t)when a 0.25-p.u. voltage sag occurs at 1.05s< t< 1.15 s.

3.1.2. Sag/Swell Detection Method

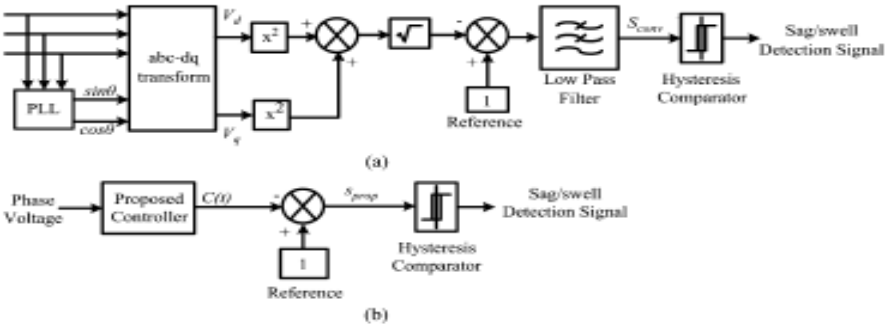

Fig 3.1.2 Block diagram of a) Conventional and b) Proposed sag detection methods

The block diagram of the transformation-based sag/swell detection method is shown. After the three-phase set of voltages is transformed into and components, the square root of the sum of squares of these components is obtained .The obtained value is subtracted from 1 (reference value) and then the absolute value of the resulting variable is filtered out with a 100-Hz low-pass filter to extract the positive-sequence component of voltage. If a negative sequence is generated by voltage sag and/or unbalance, it appears as an oscillating error in the dq -based sag detection method. To measure the positives sequence separately from the negative sequence, the dq–based method normally uses a low-pass filter that has a narrow bandwidth. But this type of filter causes a lot of phase delay or measurement delay; thus, the response time of the system tends to be lengthened.

The filtered output is subjected to a hysteresis comparator, and the output of this comparator generates the sag/swell detection signal. The signal is high when sag/swell occurs and is low otherwise. The detection method is able to detect the three-phase balanced voltage sag/swell with acceptable performance. However, the most important disadvantage of this method is that it uses three-phase voltage measurements for the detection. The method is unable to detect the voltage sag lower than a definite depth. As an instance, a single-phase-to-ground fault resulting in 15% of voltage sag cannot be determined by this method because the method uses the average of the three-phase voltage and perceives the single-phase voltage sag as an average value of 5% if the voltage sag detection limit is selected to be10% [19].To overcome the disadvantages of the sag detection method, depicted in Fig. 3 is used in this study.

With the proposed method, the controller is able to detect balanced and unbalanced voltage sags/swells without an error gives the amplitude of the tracked signal. For example, if the amplitude of the measured Phase _A supply voltage is220, the signal is obtained as continuous 1 p.u. If the amplitude falls to 165 , the amplitude of the signal falls to 0.75 p.u. presents the voltage sag/swell detection method using PLL.By subtracting the signal from the ideal voltage magnitude(1 p.u.), the voltage sag/swell depth can be detected. The comparison of this value with the limit value of 10%(0.1 p.u.) gives information as to whether voltage sag occurred.

$$S_{prop} = |1 - C(t)| \qquad (19)$$

The single-phase voltage sag initiates at 0.3 s with a duration of 0.1 s as shown in Fig. 5.1.5. The extracted component C(t) is processed in the hysteresis comparator with a band of 10%and then the sags/swells are detected within a few milliseconds. The conventional method cannot detect the sag, but the proposed method can detect the sag depth with exact certainty.

3.2 Shunt Converter Control

The shunt converter control includes the reference current computation and capacitor voltage control.

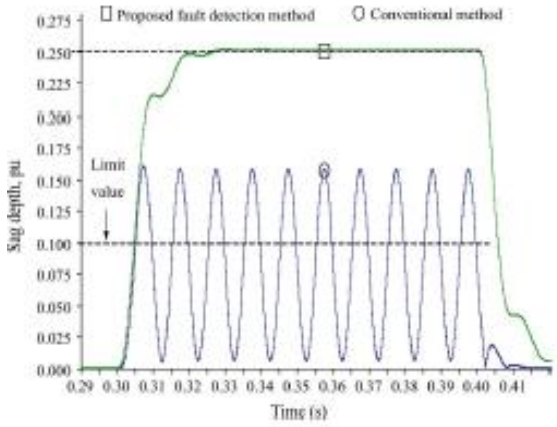

Fig a : Average depth values of sag with conventional and proposed methods.

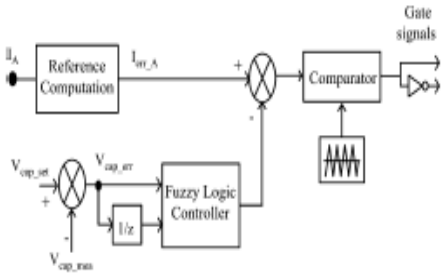

Fig b : Control block diagram of the shunt converter.

3.2.1. Reference Current Generation

For the shunt converter, A(t) corresponds to IA, and B(t) corresponds to Ierr-A as shown from Figs. and . The measurements of load currents (Il) , injected currents (If) , and dc capacitor voltage Vdc are required for control strategy of VSC_2.In the proposed method, there is no need to measure supply voltages. The required compensation signal is obtained by subtracting the FLC output from Ierr-A . The obtained signal is then compared with a carrier signal.

The equations of control signals are derived by following the same procedure as given in Section III the load current and its extracted components, such as the difference of input and synchronized fundamental component B(t), the amplitude C(t), synchronized fundamental component D(t) , and PLL signal E(t).

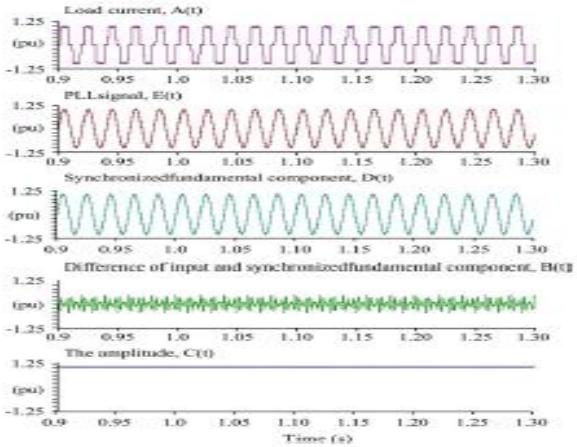

Fig 3.2.1 Load current and its extracted components

3.2.2. Capacitor Voltage Control

In the proposed method, Vcap-erris obtained from the difference of capacitor set voltage and measured capacitor voltage. Vcap-errand its rate of change are the inputs for the FLC. The output of the FLC is subtracted from the compensating current signal Vcap-err and its rate of change is defined as

$$V_{cap-err} = V_{cap-ref} - V_{cap-mess} \quad (20)$$

$$\Delta V_{cap-err} = V_{cap-err(n)} - V_{cap-err(n-1)} \quad (21)$$

The input signals are fuzzi fied and represented in fuzzy set notations by membership functions. The defined "IF … THEN…" rules produce the linguistic variables, and these variables are defuzzified into control signals. The solution of the defuzzification process results from (11)

$$U = \frac{\sum_i y_i \mu(y_i)}{\sum_a \mu(y_i)} \quad (22)$$

where denotes the crisp value of the output, represents the normalized controller output for the interval, and is the associated membership grade. The systematic approach evaluated in [19] is used for the analysis and design of proposed FLC. Membership functions are preliminarily selected as symmetrical, and the approach can be successfully applied to symmetrical membership functions. The error and error-rate memberships are divided into 5 triangular and 2 trapezoidal fuzzy sets in width, and this allows the operation to change gradually from one state to the next as shown inFig. . With this scheme, the input state of variable no longer jumps abruptly from one state to the next. A certain amount of overlap is desirable; otherwise, the controller may run into poorly defined states, where it does not return a well-defined output. Membership functions and rules are obtained from an understanding of system behavior and the application of systematic procedure and are modified and tuned by simulation performance. The rules table and the stability of the fine-tuned controller with simulation performance are justified by using the approach evaluated in [19] and deeply discussed. By following the systematic assignment procedure, a stable and optimized rule table is obtained as presented in Fig.The output of FLC is added to the current compensating signal. FLC is developed in PSCAD/EMTDC with FORTRAN codes and is applied to control the dc-link voltage for the first time without any interfacing with other simulation programs.

IV. Operation of UPQC

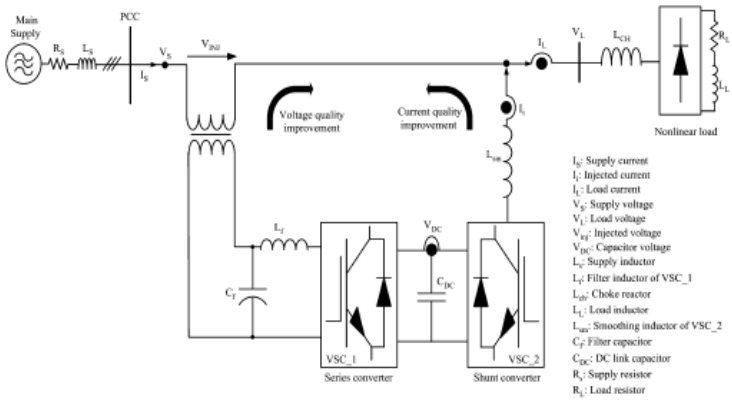

Fig 4. 0 Circuit diagram of UPQC.

The proposed UPQC system offers two operation modes as follows.

MODE 1: VSC_1 off and VSC_2 on:

When the PCC voltage is within its operation limits, VSC_1 is closed and VSC_2works as the current source [24]. During this operation of UPQC, two lower IGBTs of each phase H-bridge inverter of VSC_1 remain turned on while the two upper IGBTs remain turned off, forming a short circuit across the secondary(inverter side) windings of the series transformer through [19]. Thus, there is no need to use by pass switches across the transformers. VSC_2 suppresses the load current harmonics and regulates dc-link voltage during this mode of operation.

MODE 2 : VSC_1 on and VSC_2 on:

When the PCC voltage is out side its operating range; both VSC_1 and VSC_2 are open.VSC_1 starts to mitigate sag/swell using the energy stored in and VSC_2 continue to suppress the load current harmonics and to regulate dc-link voltage.

4.1Phase locked loop

Phase-locked loop (PLL) is a feedback loop which locks two waveforms with same frequency but shifted in phase. The fundamental use of this loop is in comparing frequencies of two waveforms and then adjusting the frequency of the waveform in the loop to equal the input waveform frequency. A block diagram of the

PLL is shown in Figure . The heart of the PLL is a phase comparator which along with a voltage controlled oscillator (VCO), a filter and an amplifier forms the loop.

If the two frequencies are different the output of the phase comparator varies and changes the input to the VCO to make its output frequency equal to the input waveform frequency. The locking of the two frequencies is a nonlinear process but linear approximation can be used to analyses PLL dynamics. In getting the PLL to lock the proper selection of the filter is essential and it needs some attention. If the filter design is understood from control theory point-of-view then the design becomes quite simple. In this short note we will discuss only the fundamentals of the PLL and how you can use nonlinear simulation and linearised approximation to get a better understanding of the PLL.

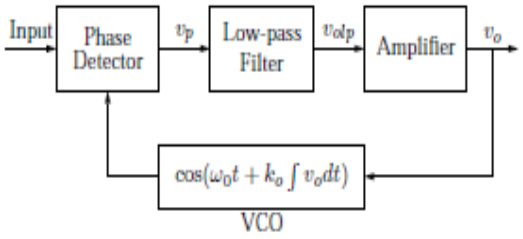

Fig 4.1: Block diagram of phase locked loop

V. Simulation and Result

The power-quality improvement capability of the UPQC system is tested through case studies using PSCAD/EMTDC. A three-phase diode-bridge rectifier is used as a harmonic current producing load with a total harmonic distortion (THD) of 24%.VSC_1 is able to compensate up to more than 30% voltage sag of the nominal voltage. The circuit parameters of the UPQC system are provided in Table I.

In this section, two test cases are presented to show the performance of the proposed UPQC under distorted supply conditions. In Test Case 1, the harmonic suppression capability ofVSC_2 is analyzed. In Test Case 2, VSC_1 is tested for single line-to-ground faults which are 70% of possible types of faults in the distribution systems [19]. The performance of VSC_1 andVSC_2 from the points of view of sag/swell detection speed, sag compensation, and harmonic suppression capabilities are investigated.

5.1 Test Case 1: VSC_1 Off and VSC_2 on

The first case presents how VSC_2 overcomes the load current harmonics with the proposed control algorithms. The nonlinear load contains lower and higher order harmonics with a total value of 24% THD. Fig. 10 shows the waveforms of supply current, load current, and dc-link capacitor voltage with FLC. The results show that a successful reduction inharmonic of the supply current is obtained. A nonlinear load current with 24% THD is approximately reduced to 4% with a PI controller and 3.7% with FLC. The THD of is reduced from 24% to less than 4%, and the distortion is within the limits prescribed by the standards. The fuzzy-logic-controlled dc-link capacitor voltage is nearly kept at 650 . During Test Case1, the THD of the load voltage (1.43%) is below the 5% limit recommended by IEEE Standard 519 [33]. THD contents of supply and filtered currents for Phase Aare presented in Table II. The amplitudes of characteristic harmonics (5th, 7th, 11th, and 13th) are high in the load current. The APF injects the required compensation current to this article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

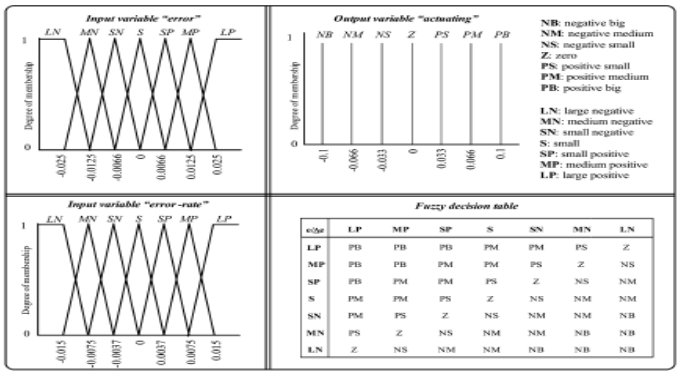

Fig 5.1 Membership shapes of I/O fuzzy sets and assignment of the control rules.

System quantity	Supply voltage (Vs) Frequency Impedence	380 Vrms (line to line) Phase-A, 1.4%THD Phase-B, 1.4%THD Phase-C, 1.4%THD 50Hz 0.004Ω+j0.016Ω
Series converter VSC-1	Filter inductor(Lf) Filter capacitor (Cf) Injection transformer Switching frequency	8mH 36μF 5:1 turns ratio 5kHz
Shunt converter VSC-2	DC link capacitor Cdc Reference voltage Smoothing inductor Lsm Choke reactor Lch Switching frequency	1100μF 650 Vdc 15mH 3mH 5KHz
Nonlinear load	Load impedence	40Ω+j10Ω

Table 1: Simulation parameters.

the system, and the amplitudes of characteristic harmonics are minimized in the supply current.

5.2 Test Case 2: VSC_1 on and VSC_2 on

The second case presents how VSC_1 copes with the single phase sag with 20% between 1s<t<1.6 s. The fault initiates at start= 1 s and is detected at detect= 1.0054 s. With the proposed detection method, the starting time of the fault is detected within 0.0054 s as shown in Fig. 11.
Fig. shows the view of supply (Vs) and load voltage (VL) waveforms before and during the voltage sag.

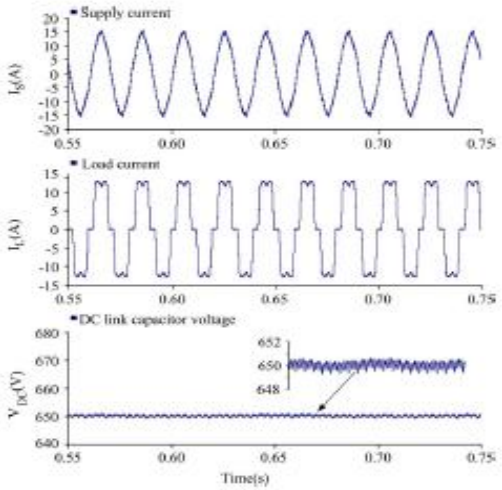

Fig 5.2: Waveforms of the supply current, load current, and dc-link capacitor voltage.

The sag/swell detection unit quickly determines the start and end times of the sag. Once voltage sag is detected, VSC_1 enters into on-mode and starts to inject the required missing voltage to the grid. During the fault, the rams of the supply voltage is reduced 176Vrms to from 220Vrms. The load voltage magnitudes maintained under 10% voltage limits (THD 1.64%) with the help of rapid and effective compensation capability of VSC_1. Fig. shows the rms values of Vs and VL before and during the fault. VSC_2 continues to suppress the load current harmonic during Test Case 2.

During voltage sag, VSC_1 injects the required missing voltage but the THD value of load voltage goes from 1.43% to1.64%. This can cause the additional harmonics to flow into the load current. Fuzzy-logic-controlled VSC_2 overcomes this situation. FLC performs superior performance than the PI controller during fault. The supply current THD is approximately reduced to 13% with the PI controller and 3.65% with FLC, respectively. During fault, the THD of the load (THD1.64%) voltage is below the 5% limit and the supply current is below the 5% limit recommended by IEEE Standard 519.is nearly kept at 650 before the voltage sag .Switching losses and the power received from through the series converter can fluctuate the average value of during the fault. The fuzzy-logic controller keeps the value almost at 650 during the sag. The amplitudes of characteristic harmonics (5th, 7th, 11th, and 13th) are minimized in the supply current with APF.

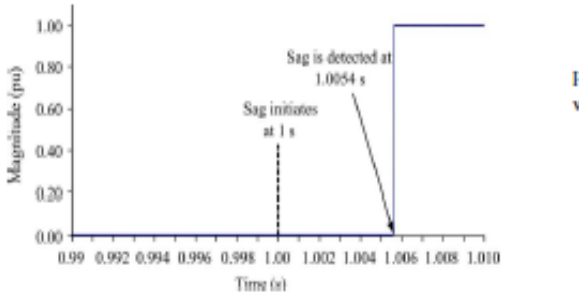

Fig 5.3: Voltage sag detection signal of the proposed method.

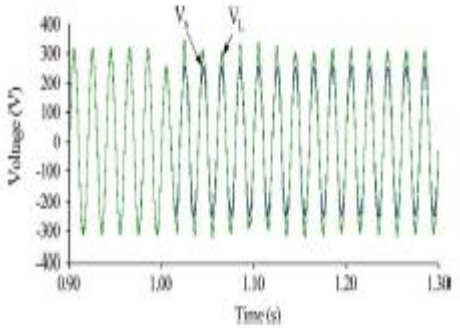

Fig 5.4: waveforms of the supply and load voltages.

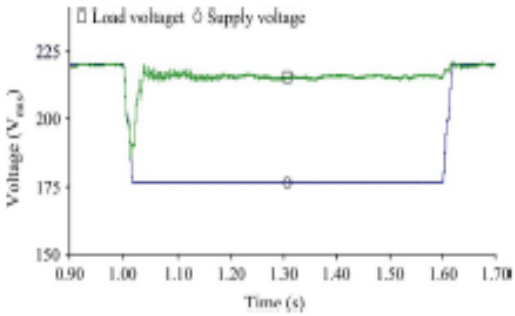

Fig 5.5: RMS values of the supply and load voltages

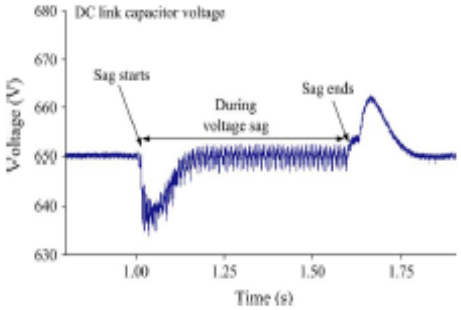

Fig 5.6: Variation of the dc link capacitor voltage

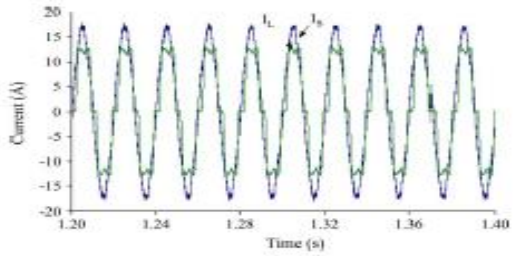

Fig5.7: Current waveforms of Il and Is during voltage sag

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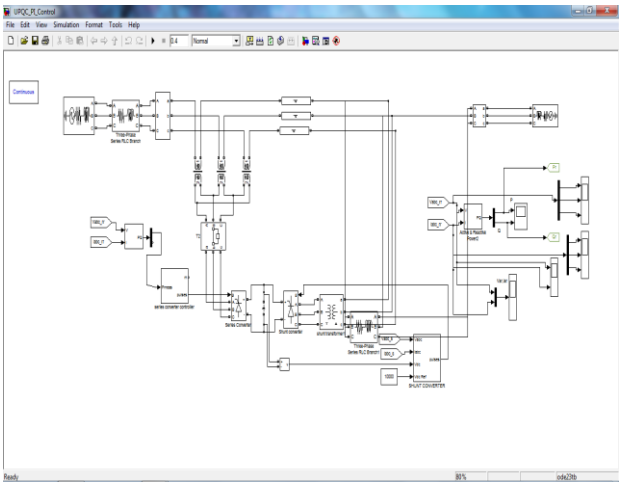

Fig 5.8: Snap shot of UPQC circuit.

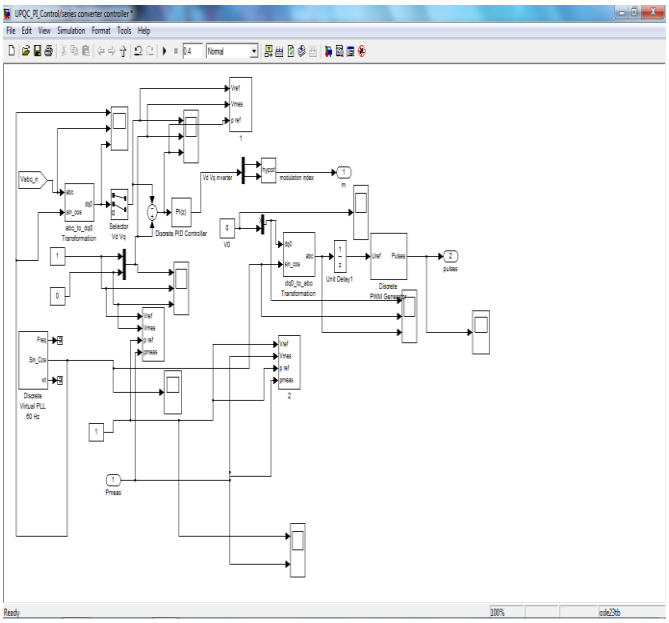

Fig5.9: Snap shot of series converter circuit.

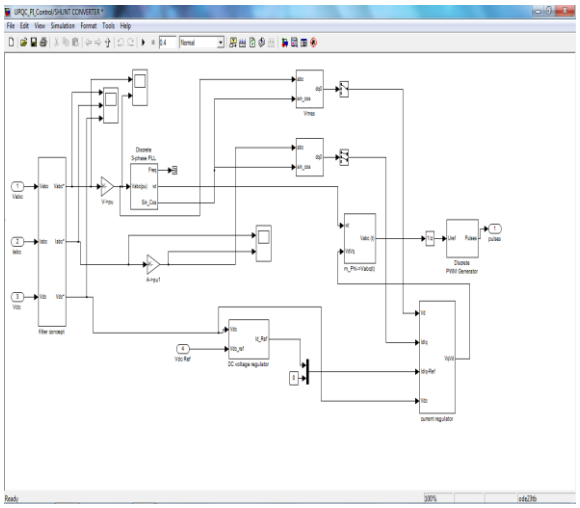

Fig 5.10: Snap shot of shunt converter circuit.

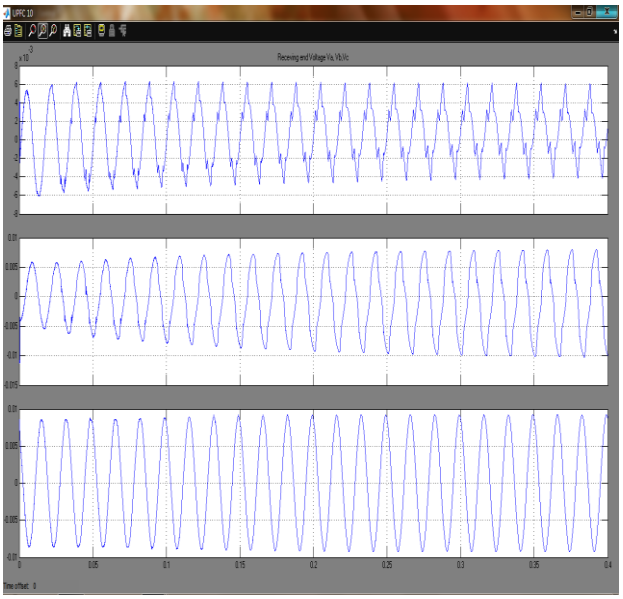

Fig 5.11: Snap shot of receiving end voltage waveform.

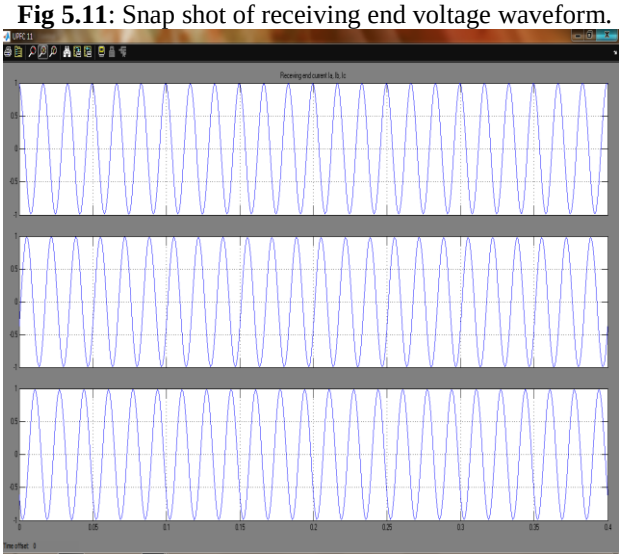

Fig 5.12: Snap shot of receiving end current waveform.

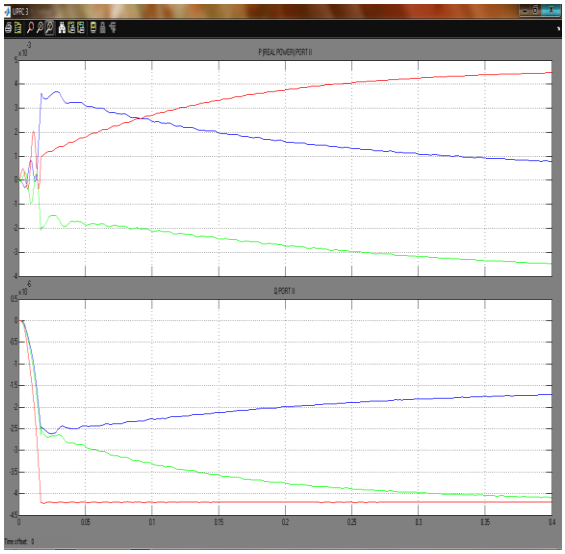

Fig5.13: Snap shot of Variation of the dc link capacitor voltage waveform.

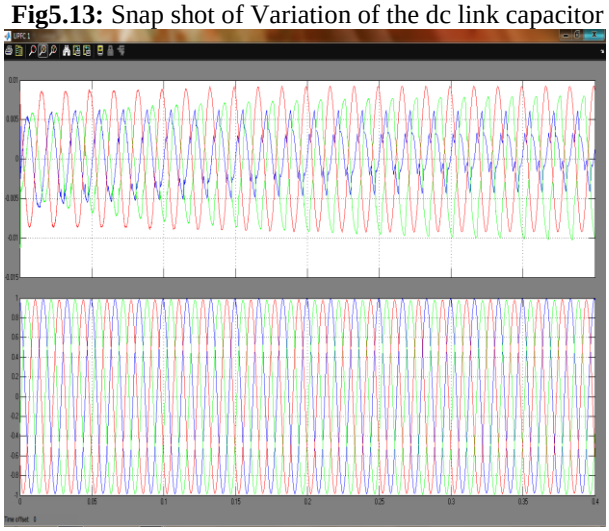

Fig5.14: Snap shot of current and voltage waveform**.**

VI. Conclusion

A novel controller for the unified power-quality conditioner is introduced and analyzed by controlling voltage–source converters (VSC_1 and VSC_2) based on enhanced PLL and nonlinear adaptive filter algorithms and dc-link voltage with a fuzzy-logic controller. New functionality is added to the UPQC system to quickly extract the reference signals directly for load current and supply voltage with a minimal amount of mathematical operands. The computation method is simpler than for other control algorithms of reference extraction. The number of parameters to be tuned has also been reduced by the use of the proposed controller. This paper presents an effective and fast voltage sag/swell detection method for unbalanced faults. The performance of the proposed UPQC and controller for PQ improvement is tested through the case study simulations (e.g., voltage sag and harmonic producing load using PSCAD/EMTDC). The case results meet the regulations of IEEE Standard 519 and demonstrate that the proposed UPQC system provides simultaneous mitigation of a variety of PQ problems.

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