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Reduction of Subthershold Leakage Current by Technology Scaling

Ms. Sunita Beniwal, Ms. Sudha Rani

Abstract

The driving force for the semiconductor industry growth has been the elegant scaling nature of CMOS technology. In future CMOS technology generations, supply and threshold voltages will have to continually scale to sustain performance increase, limit energy consumption, control power dissipation, and maintain reliability. These continual scaling requirements on supply and threshold voltages pose several technology and circuit design challenges. One such challenge is the expected increase in threshold voltage variation due to worsening short channel effect,supply voltage scaling, control of *die-to-die threshold voltage variation* becomes critical for maintaining high yield. An analytical model will be developed for existing circuit technique that adaptively biases the body terminal of MOSFET devices to control this threshold voltage variation. Based on this model, recommendations on how to effectively use the technique in future technologies will be presented. in future CMOS systems. Therefore, it becomes imperative to accurately predict and minimize leakage power of such systems, especially with increasing *within-die threshold voltage variation*. Finally, due to different processing steps and short channel effects, threshold voltage of devices of same or different polarities in the same neighborhood may not be matched. This will introduce mismatch in the device drive currents that will not be acceptable in some high performance circuits.

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I. Introduction

The ever shrinking size of the MOS transistors that result in faster, smaller, and cheaper systems have enabled ubiquitous use of these chips. Among these semiconductor chips, a prevalent component is the high-performance general-purpose microprocessor . The timeline on technology scaling and new high performance microprocessor architecture introductions in the past three decades [2]. This trend holds in general for other segments of the semiconductor industry as predicted by Moore's law [3].

In 1965, Gordon Moore showed that for any MOS transistor technology there exists a minimum cost that maximizes the number of components per integrated circuits. He showed that a result of continuous miniaturization transistor count would double every 18 months 53% compound annual growth rate over 45 years No other technology has grown so fast so long. Transistors become smaller, faster, consume less power, and are cheaper to manufacture. He also showed transistor dimensions are shrunk (or scaled) from one technology generation to the next, as shown in

Figure 1

Historically, technology scaling resulted in scaling of vertical and lateral dimensions by 0.7X each generation resulting in delay of the logic gates to be scaled by 0.7X and the integration density of logic gates to be increased by 2X. There were two distinct eras in technology scaling – constant voltage scaling and constant electric field scaling.

Constant voltage scaling era (*First two decades*)

Technology scaling and new architectural introduction in this era happened every 3.6 years. Technology scaling should scale delay by 0.7X translating to 1.4X higher frequency. However, frequency scaled by 1.7X with the additional increase primarily brought about by increase in the number of logic transistors. As we know that the number of logic transistors increased by 3.3X in each of the new introductions. Technology scaling itself would have provided only 2X – the additional increase was enabled by increase in die area of about 1.5X every generation [4]

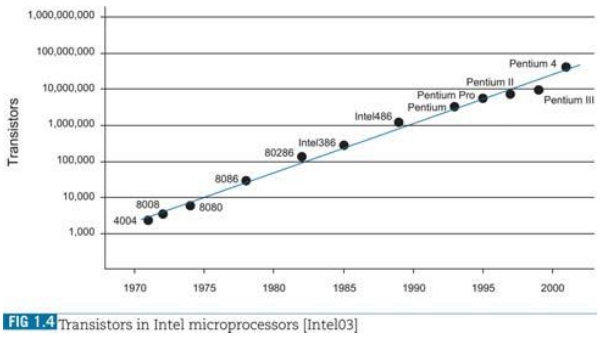

Figure 1: Moore's law.

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Constant electric field scaling era
(*Past decade*)

Technology scaling and new architectural introduction in this era happened every 2 years along with voltage scaling of 0.7X. As always technology scaling should scale delay by 0.7X translating to 1.4X higher frequency, but frequency increased by 2X in each new introduction. The additional increase in frequency was primarily brought by decrease in logic depth through architectural and circuit design advancements. The number of logic transistors grew only by about 2.1X every generation, which could be achieved without significant increase in die area. Since switching power is proportional to Area x □/distance x Vdd x Vdd x F, it increased by (1 x 1/0.7 x 0.7 x 0.7 x 2 =) 1.4X every generation. Although the die size growth is not required for logic transistor integration, it is important to note that the total die area did continue to grow at the rate of 1.5X per generation [4] due to increase amount of integrated memory.

In the past decade, technology and new architecture product cycles reduced from 3.6 years to 2 years. From an operational perspective, this requires concurrent engineering in product design, process design, and manufacturing supply lines [5]. The past decade also required supply voltage scaling imposed by oxide reliability and the need to slow down the switching power growth rate. From the process design stand point supply voltage scaling requires threshold voltage scaling [6, 7] so that the technology scaling can continue to provide 1.4X frequency increase. To prolong the tremendous growth the industry has experienced in the past four decades threshold voltage scaling and concurrent engineering has to continue. These requirements pose several challenges in the coming years including increase in process variation, worsening interconnect RC delay, and increase in sub-threshold, gate, and tunneling leakage components. Conventionally, CMOS technology has been scaled to provide 30% smaller gate delay with 30% smaller dimensions, resulting in CMOS systems operating at about 40% higher frequency in half the area with reduced energy consumption.

Technology scaling and subthreshold leakage current (Ioff). Variation

Today transistors with minimum dimension of 130 nm are used and after that scaling cannot go on forever because transistors cannot be smaller than atoms .With technology scaling, the MOSFET's channel length is reduced. As the channel length approaches the source-body and drain-body depletion widths, the charge in the channel due to these parasitic diodes become comparable to the depletion charge due to the MOSFET gate-body voltage [11], rendering the gate and body terminals to be less effective. As the band diagram illustrates in Figure 2, the finite depletion width of the parasitic diodes do not influence the energy barrier height to be overcome for inversion formation in a long channel device. However, as the channel length becomes shorter both channel length and drain voltage reduce this barrier height. This two dimensional effect makes the barrier height to be modulated by channel length variation resulting in threshold voltage variation as shown in Figure 3.The amount of barrier height lowering, threshold voltage variation, and gate and body terminal's channel control loss will directly depend on the charge contribution percentage of the parasitic diodes to the total channel charge. Figure 4 shows measurements of 3□ □threshold voltage variations for three device lengths in a 0.18-□m technology confirming this behavior. It is essential to mention that in sub-micron technologies variation in several physical and process parameters lead to variation in the electrical behavior of the MOS device and variation in the electrical behavior manifested as threshold voltage variation because of parameter variation. In addition, the threshold voltage variations addressed here are due to short channel effect in scaled MOS devices and not on threshold voltage variation due to random dopant fluctuation effect. Random dopant fluctuation effect is expected to be one of the significant sources of threshold voltage variation in devices of small area [12].

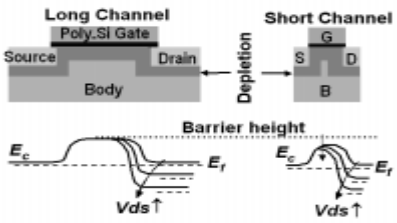

Figure 2: Barrier height lowering due to channel length reduction and drain voltage increase in an nMOS.

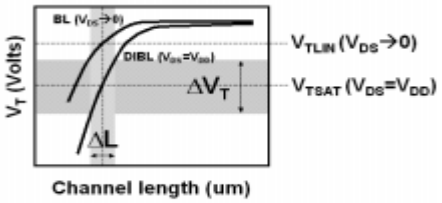

Figure 3: Barrier lowering (BL) resulting in threshold voltage roll-off with channel length reduction. Drain induced barrier lowering (DIBL) reduces threshold voltage for short channel devices and increases threshold voltage roll-off. For short channel devices channel length variation (□L) translates to threshold voltage variation (□VT)

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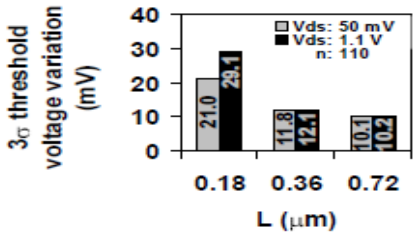

Figure 4: Dependence of threshold voltage variation on channel length and drain voltage; n is the number of MOS device samples measured.

As we know that in order to maintain the performance increase trend with technology scaling threshold voltage would have to be scaled along with supply voltage. However, reduction in threshold voltage increases the sub-threshold leakage current significantly. Relationship between threshold voltage and sub-threshold leakage is illustrated in Figure 5. Typically, reduction in threshold voltage of about 85 mV, as shown in Figure 2-4, will increase the sub-threshold leakage current by 10X.

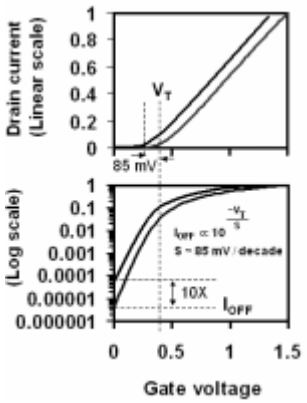

Figure 5: Relationship between threshold voltage (Vt) and sub-threshold leakage current (Ioff).

As mentioned above switching power increases by 1.4X per generation. With scaling of threshold voltage sub-threshold leakage power will increase at a very rapid rate due to its strong dependence on the threshold voltage. Figure 6 illustrates the comparison between the increase in the switching power and sub-threshold leakage power with technology scaling. As it is evident from the figure sub-threshold leakage power will be comparable to the switching power in the immediate future. This 'inefficient' leakage power manifests itself as active leakage that influences the total power budget during operation and as standby leakage that influences the battery life of hand held systems. It therefore becomes important to not only reduce sub-threshold leakage power but also accurately estimate it.

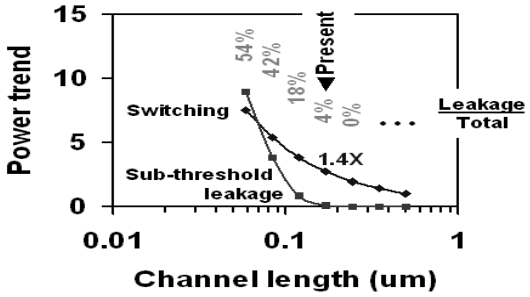

Figure 6: Trend in sub-threshold leakage and switching power with technology scaling

With supply and threshold voltage scaling, control of threshold voltage variation becomes essential for achieving high yields and limiting worst-case leakage [13]. Maintaining good device aspect ratio, by scaling gate oxide thickness is important for controlling threshold voltage tolerances [7]. With the silicon dioxide gate dielectric thickness approaching scaling limits due rapid increase in gate tunneling leakage current [14, 15] researchers have been exploring several alternatives, including the use of high permittivity gate dielectric, metal gate, novel device structures and circuit based techniques [16, 17]. The use of high permittivity gate dielectric will result in thicker and easier to fabricate dielectric for iso-gate oxide capacitance with potential for significant reduction in gate leakage. Identification of a proper high permittivity dielectric material that has good interface states with silicon along with limited gate leakage is in progress [16]. However, it has also been shown that use of high permittivity gate dielectric has limited return [17]. Use of metal gate prevents poly-depletion resulting in a thinner effective gate dielectric. However, identification of dual metal gates to replace the n+ and p+ doped polysilicon is essential to maintain threshold voltage scaling. In addition, novel device structures such as self aligned double gate planar MOSFETs provide better device aspect ratio Other than material and device based solutions, circuit design solutions such as threshold canceling logic and adaptive body bias enable supply and threshold voltage scaling.

Conclusion

One of the important device parameters that impact the design of circuits is its threshold voltage. Technology scaling and moore law are driving force behind semiconductor industry. Since the variation in the threshold voltage is expected to increase with scaling, it is imperative to understand the nature of its impact, models to predict the magnitude of impact, and techniques to reduce its impact.

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