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Integrated Random noise source using 45nm VLSI Technology

Sathyanarayana R
VTU extension centre,
UTL Technologies Ltd, Bangalore, Karnataka, India

----------Abstract----------

The word "noise" is in everyday use, is any unwanted sound that can be heard. Electrical noise has significantly different meaning. Electrical noise is a current or voltage signal that is unwanted in an Electrical / Electronic circuit. The real time signal is sum of unwanted noise and desired signal. The noise can be of two types. Discrete and random. Each noise can be generated with various techniques and methods. But, the random noise source has many useful applications in Electronic test and measurement, embedded systems, computing and Communication systems

Design and implementation of integrated random noise source (IRNS) is based on the concept, random noise source can be a resistor. The true random noise can be generated due to random movement of electrons. This noise amplitude is very small. This noise is being amplified by an amplifier like Operational amplifier and then comparator compares the amplified noise signal and generates digital signal, which is true random. This true random noise can be used to generate random numbers, which can be used applications such as cryptography.

In this project, a random noise source is developed using 45nm technology. Design and implementation of Resistor, Operational amplifier and Comparator is done and integrated them. The integrated IRNS is tested by simulation. The layout of each component is done and integrated & tested to complete IRNS 45nm .

Keywords-- *-IRNS, OP. Amp, comparator, simulation.*

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I. Introduction

A random noise source has many useful applications in Electronic test and measurement, Embedded systems, computing and communication systems. The noise can be of two types. Discrete and random. Each noise can be generated with various techniques and methods. Initial discrete noise source is controlled by P-N junction operating in Avalanche mode. Random noise by resistor , due to random movement of electrons.

The new development in computing and Telecommunication , needs data security. So data security and Encryption are new areas of research and development. And applications. Many Encryption Standards have been developed. Encryption and Decryption uses various algorithms and keys. They use random binary numbers. A digital noise source that can provide continuous true random numbers are very useful in encryption of video , voice and other types of data. A discrete noise source has a no. Of limitations in terms of size, supply voltage , cost etc in micro electronic design. So an ideally , a noise source integrated directly on the same substrate as the digital VLSI application requiring random numeric input. This needs a design, development and implementation of an integrated analog/ digital random noise source.

The specifications of IRNS are described in this section. They are input specifications, output specifications and functional & parametric specifications. There is no specific external input to IRNS. The random noise is generated depends on random motion of electron by noise generating component. The value of noise generated by resistor is equal 4KTR, where K is Boltzmann's constant, T is Temperature in degree K and R is the resistance in ohms. The output peak to peak noise amplitude is 100m V(analog 1/f noise frequency is < 5Hz.]

II. Design , Analysis And Implementation

The Design , analysis and implementation of IRNS is divided into its components design and implementation. The components are integrated into IRNS.

The various components and tasks of IRNS.

1. Design & implementation of resistor..
2. Design & implementation of operational amplifier..
3. Design & implementation of comparator.

The components implemented are tested by Simulation and integrated to IRNS.. The IRNS is tested simulation for functionality and noise simulation several times. This ensures the noise generated is random.

The block diagram of the IRNS is as shown in fig 1.

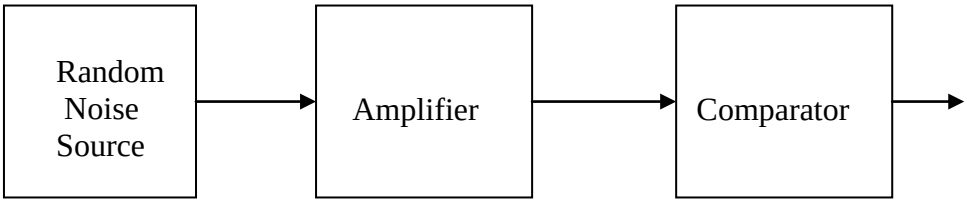

Fig 1. Block diagram of IRNS

The Random noise source value is calculated based on min. input required at the input of amplifier, Bandwidth and gain of amplifier.

A two stage amplifier is used to amplify noise generated. by resistor. The amplifier has the following components i) Current mirror for providing bias current. ii) Differential , high gain stage, with one input grounded (inverting terminal) iii) Output stage , which is to increase the swing. The output of amplifier is analog noise source, which should have minimum value of 100mvp-p.

The comparator converts analog noise to digital bit The comparator used in IRNS is two stage open loop comparator. The comparator has also has current source , differential stage with one of (inverting) grounded, and output stage.

II. Verification And Simulation:

The verification is the process of ensuring, verifying the design is meeting the requirements. IRNS is tested by means of simulation, First at component level and then at integrated system level. The operational amplifier and comparators are tested for transient, ac and dc responses. Then all 3 components are integrated and subject to noise simulation. Noise simulation is done several times to check whether noise generated is random.

III. Conclusion & Future Work

The IRNS is implemented and tested by simulation. The simulation is carried out at component level first and then at integrated system level for its functionality. The results found to be meeting the functional requirements of IRNS.

The functionality tested IRNS , tested for noise simulation and results are analysed. The simulations are carried out to verify the noise generated are truly random and meets the IRNS requirement. The analysis of graphs of noise waveforms of several iteration together indicates that the results of noise generated are meeting the concept and requirements of IRNS.

The following future works are possible to extended the work on IRNS.

1) Post processing of Digital output of IRNS.
2) Von-Neumann corrector
3) Cryptography applications.

The noise generated by resistor is truly random and has very high or infinite bandwidth. The effect of other components and B.W may limit the truly randomness. To eliminate such effects, both Post processing circuits and Von-Neumann corrector circuits are used. Several tests can be carried out on output to ensure it is truly random. There is a loft of scope for research in these areas.

The application of the random numbers generated by IRNS can be used in the several areas such as Cryptography. IRNS provides foundation for several such applications.

IV. Aoknowledgement

The IRNS is implemented and tested by simulation. I acknowledge Dr. P.V Ananda Mohan, Senior technical expert of ECIL and Dr. V. Ventkateswarlu, Principal ,UTL for their guidance and Dr. Siva yellampalli, Professor UTL for suggestion and UTL labs for providing facility during this IRNS development & implementation. .

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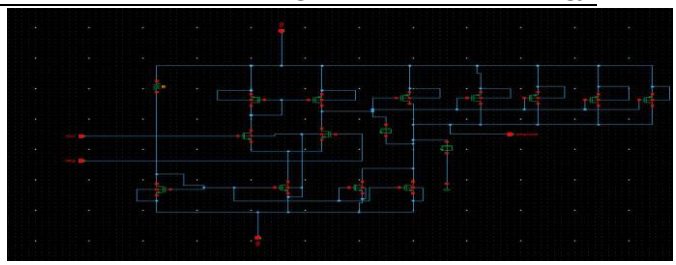

Fig 2 : IRNS 45nm Op.Amp

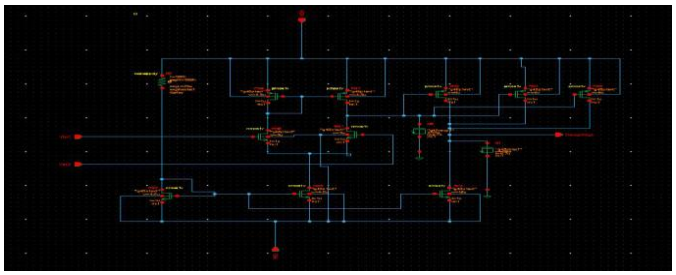

Fig 3 : IRNS 45nm Comparator

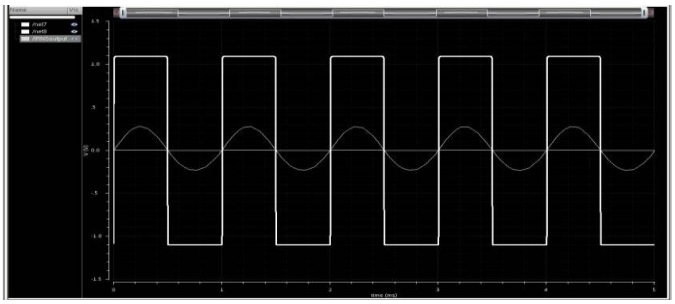

Fig 4 : 45nm integrated IRNS Functionality

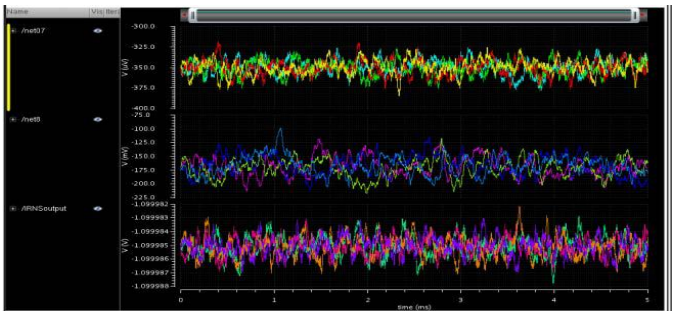

Fig 5 : Noise wave form of IRNS 45nm

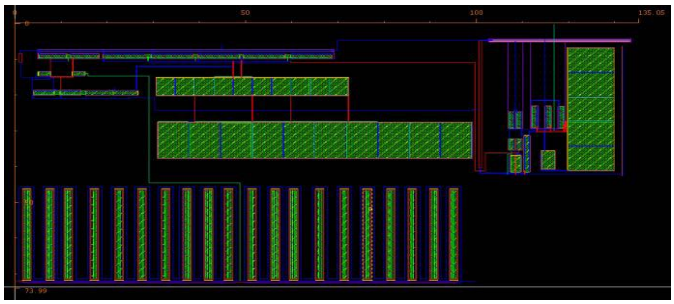

Fig 6 : Layout of integrated IRNS 45nm