The International Journal of Engineering And Science (IJES)
||Volume|| 2 ||Issue|| 01 ||Pages|| 191-193 ||2013||
ISSN: 2319 – 1813 ISBN: 2319 – 1805

Effect of Scaling On Operation of Low Voltage OTA

[1]Anjali Vijay Khare, [2]Dipak Dahigaonkar
[1, 2]*Department of Electronics, RKNEC, R.T.M.Nagpur University,*

----------ABSTRACT----------

The increasing demand for higher data rate contributes in enhancing overall growth of digital systems. However, an analog system continues to be a vital part of electronics sensor circuits. Thus every DSP consists of both analog and digital sections. The need to lower down the power consumption in these systems has led to a scaling down of most technologies. The Current-mode design techniques in analog circuits results in the enhancement of bandwidth and linearity. One of the important building blocks in current-mode analog signal processing is the OTA, which is basically a voltage to current converter. This paper deals with design and analysis of single output Operational Transconductance Amplifier (OTA) in submicron CMOS process technology (which was earlier done in 350nm technology). Simulations have been carried out in Hspice-Synopsys and Awanwaves. This paper also covers effects of scaling on various parameters such as power dissipation, total harmonic distortion , bandwidth etc. of the single output OTA in various CMOS process technology.

Keywords - *Operational Transconductance Amplifier, Total Harmonic Distortion, CMOS, CMOS process technology, Low voltage/ Low power.*

Date of Submission: 26, December, 2012 ⟺ Date of Publication: 11, January 2013

I. INTRODUCTION

Operational Transconductance amplifiers (OTAs) are important building blocks for various analog circuits and systems. Depending on system needs, an OTA must satisfy many design requirements. As CMOS technologies evolves the supply voltage decreases and device characteristics deteriorate. CMOS provides the highest analog-digital on-chip integration. At present times, a typical Applications Specific Integrated Circuit (ASIC) contains about 80% digital and 20% analog circuitry. The digital circuits are more robust with better performance. However, digital circuits are inherently power hungry. This has motivated the continual decrease in the feature size of silicon technology and the supply voltage. The operational transconductance amplifier topology which is a single output OTA was simulated in 350nm technology .These paper presents the simulation and results of the single output OTA in 90nm technology. The main objective of this paper is to study the effects of the scaling on the operational transconductance amplifier parameters such as power dissipation, Total harmonic distortion (THD), bandwidth etc.

Bandwidth (or settling time), accuracy (offset, noise, and gain), and power consumption are three of the most important properties of the analog design. However, they cannot be satisfied simultaneously. In order to achieve higher bandwidth (or less settling time), accuracy is often sacrificed and more power consumed. It is the analog designer's task to make the tradeoffs between bandwidth and accuracy at minimum power consumption. Less power is especially important in this "portable" era.

II. LV OTA DESIGN

A widely used approach in design of low voltage circuits is to reduce the number of transistors between the supply voltage and ground. This approach led to the design of an OTA topology depicted in [1] known as basic transconductor stage, which is not only very simple in design but also works at really low voltages. The output current is given by:

$$I_0 = g_m . V_{in} \qquad (1)$$

Although it possesses good frequency response, the topology carries the disadvantage of lack of tunability & limited linearity.

Fig. 1 shows the circuit diagram for single output OTA. This topology utilizes a variant of cross-coupled cell to build the transconductor. In order to realize a low voltage circuit just two MOSFETs have been used between the power supply and ground. The circuit is also tunable. The differential input is fed at the gates

of M0 and M8. Vb is the control voltage, which adds the proper tunability to the circuit. The output current Io is given by:

$$I_0 = 2k_n\alpha^2(V_1 - V_2)(2V_{tn} - V_b) \qquad (2)$$

and the transconductance gm is given by:

$$g_m = 2k_n\alpha^2(2V_{tn} - V_b) \qquad (3)$$

Where K_n and V_{tn} have their usual meaning , V_1-V_2 is the differential input, α is a scaling factor for the series connected transistors and V_b is a bias voltage that controls the transconductance gm .

The trasconductance g_m of an OTA is a function of OTA operating point, input voltage, output current, and temperature and process parameters. The output current in OTA is expanded in terms of Taylor series which has dc component, a fundamental frequency and other higher order harmonics which can cause significant distortion. The distortion can be reduced using various linearization techniques.

III. SCALING AND EFFECT OF SCALING

Reducing the channel length of a MOSFET can be described in terms of scaling theory. A scaling parameter S (S < 1) is used to scale the dimensions of a MOSFET. The value of S is typically in the neighbourhood of 0.7 from one CMOS technology generation to the next. For example, if a process uses a Vdd of 2V, a next generation process would use a Vdd of 1.4V.

The main benefits of scaling are smaller device sizes and thus reduced chip size (increased yield and more parts per wafer), lower delays, allowing higher frequency operation, reduction in power dissipation. Associated with these benefits are some unwanted side effects referred to as short channel effects such as Hot carriers, Oxide breakdown, Drain Induced Barrier lowering (DIBL), Substrate Current-Induced Body Effect (SCBE), Gate tunnel current.

I. FIGURES AND TABLES

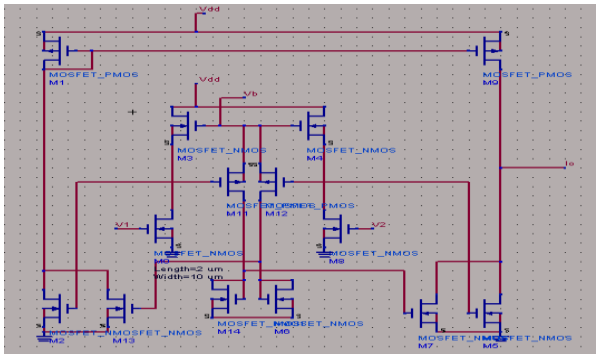

Fig. 1 Single output Operational Transconductance Amplifier

TABLE I
ASPECT RATIOS OF THE TRANSISTORS IN OTA

Transistor	W/L ratio (180nm)	W/L ratio (90nm)
M3, M4	4u/180n	2u/90n
M0-M2, M5-M14	2u/180n	1u/90n

Table-I presents the aspect ratios of the transistors used in the Dual input single output OTA. Simulation results of the OTA were obtained using a HSPICE Level 49 model. The aspect ratios of the transistors have been selected so as to ensure optimum performance.

Fig. 2 shows the ac analysis of the OTA , an ac sweep was conducted for the frequency response of this OTA topology. The current bandwidth was found to be 123MHz , 5.46 GHz and 15.4 GHz approximately for 350nm , 180nm and 90nm respectively.

The transconductance gain was found to be -80.43 dB for 350nm and it increases when the technology is nanotechnology. Table –II gives the transconductance values of the OTA in dB.

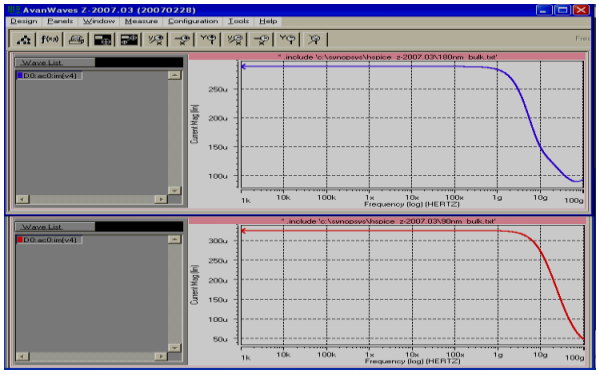

Fig. 2 A.C. analysis of OTA in 180nm &90nm

Fig. 3 and Fig. 4 shows the transient analysis of the OTA, when conducting the transient analysis the circuit was found to be stable. For a input of 100mV at a frequency of 1MHz, the distortion produced by the circuit is reduces to 0.0566 for 90nm technology.

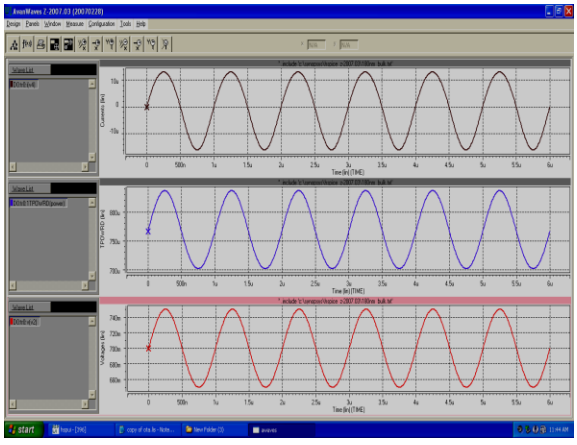

Fig. 3 Transient Analysis of OTA in 180nm

Fig. 3 is the transient simulation in 180nm which shows the applied input voltage, output current and power consumption during transient simulation maximum value is 850uWatts and minimum is 700uWatts.

Fig. 4 is the transient simulation in 90nm which shows the applied input voltage , output current and power consumption during transient simulation maximum value is 770uWatts and minimum is 670uWatts.

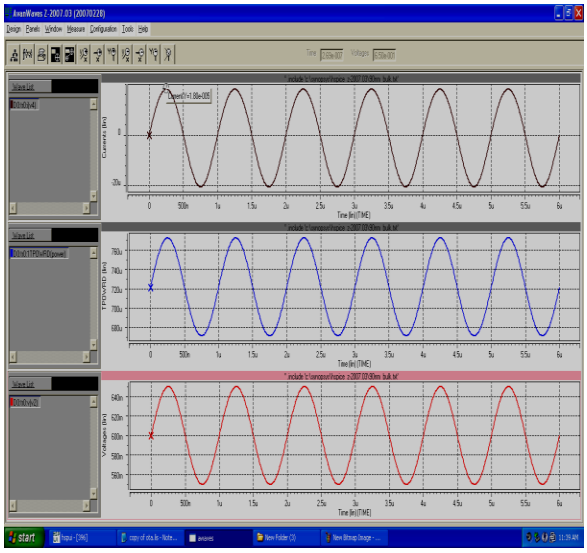

Fig. 4 Transient Analysis of OTA in 90nm

TABLE II
PERFORMANCE SPECIFICATIONS OF SINGLE OUTPUT OTA

CMOS process (nm)	Power (mW)	Iopp (uA)	T.H.D (%)	F_{3dB} (GHz)	Gain (dB)
350	3.369	20	0.2786	0.123	-80.43
180	0.7669	28.8	0.0966	5.46	-70.12
90	0.7214	38	0.0566	15.4	-68.31

IV. CONCLUSION

The single output OTA topology is scaled down in 180nm and 90nm with supply voltage 1.5V and 1.3V (LV) respectively. The Aspect ratios of the corresponding transistors is given in Table-I. The power dissipation at 180nm is found to be 0.7669mW and in 90nm it is found to be 0.7214mw. The output current swing obtained in 180nm (124µ -136µ) is less than the 90nm (215µ -250µ) technology. Thus it can be concluded that in 90nm the output current obtained is more with less power dissipation as compared to two other technology. From Table-II the power dissipation in 350nm is 3.369mW which gradually decreases as we are shrinking the process technology.

Output current, Current Bandwidth and Transconductance gain obtained is enhanced in 90nm. Power consumption is reduced (LV/LP) and total harmonic distortion is also reduced. Hence the circuit performance is enhanced as we are shrinking the technology and Low voltage /Low power circuits are preferred for the enhanced performance it provides.

REFERENCES

[1]. Majumdar D. M.Sc. Thesis (2001). Design of Low Voltage Operational Transconductance Amplifiers for Analog Applications. Electrical and Computer Engineering, Calgary, University of Calgary: 1-121.

[2]. K. Bult and H. Wallinga, "A Class of Analog CMOS Circuits Based on the Square-Law Characteristics of a MOS Transistor in Saturation," IEEE J. of Solid-State Circuits, vol. SC-22, pp. 357-365, June 1987.

[3]. X. Zhang, B. J. Maundy, E. I. El-Masry and I. G. Finvers, "A Novel Low-Voltage Operational Transconductance Amplifier and its Applications", International Symposium on Circuits and Systems, May 2000, pp. 661-664.

[4]. B.J. Maundy, I.G. Finvers and P. Aronhime, "Cross Coupled Transconductance Cell with Improved Linearity Range", International Symposium on Circuits and Systems, May 2000, pp. 157-160.

[5]. S. Pavan and Y. P. Tsividis, High Frequency Continuous Time Filters in Digital CMOS processes. Norwell: Kluwer Academic Publishers, 2000.

[6]. S. Dupuie and M. Ismail, "High Frequency CMOS Transconductors", in Analog IC Design The Current Mode Approach, Edited by C. Toumazou, F. J. Lidgey, and D. Haigh, Chapter 5, Peter Peregrinus Ltd., 1990.

[7]. Claudio Fiegna, "The effects of scaling on the performance of small-signal MOS amplifiers" Solid-State Electronics 46 (2002) 675–683.

[8]. Xunyu zhu "Impacts of cmos scaling on the analog design" 2005.